Robust Hybrid TFET-MOSFET Circuits in Presence of Process Variations and Soft Errors

Maedeh Hemmat, Mehdi Kamal, Ali Afzali-Kusha, Massoud Pedram

▶ To cite this version:

HAL Id: hal-01675198

https://inria.hal.science/hal-01675198

Submitted on 4 Jan 2018

Robust Hybrid TFET-MOSFET Circuits in Presence of Process Variations and Soft Errors

Maedeh Hemmat[1], Mehdi Kamal[1], Ali Afzali-Kusha[1], Massoud Pedram[2]

[1]School of Electrical and Computer Engineering, University of Tehran
`{m.hemmat, mehdikamal, afzali}@ut.ac.ir`
[2]Department of Electrical Engineering, University of Southern California
`pedram@usc.edu`

Abstract. In this work, to improve the timing yield of Tunnel Field Effect Transistor (TFET) circuits in the presence of process variations as well as their soft-error resiliency, we propose replacing some of TFET-based gates by MOSFET-based ones. The effectiveness of the proposed TFET-MOSFET hybrid implementation of the circuits are investigated by first studying the impacts of the process variation on the performances (*I-V* characteristics) of both homojunction InAs TFETs and MOSFETs. Next, to analyze the soft error rate of the circuits, the particle hit-induced transient current profiles of these devices are extracted. Based on these studies, a hybrid TFET-MOSFET circuit design approach which improves the reliability and soft-error resiliency compared to those of pure TFET-based circuits is suggested. Finally, the efficacy of the design approach is investigated by applying it to some circuits of ISCAS'89 benchmark package.

1 Introduction

Todays, almost all of the digital circuits are based on the MOSFET transistors. However, owing to the increase in the usage of portable devices, reducing the power consumption of digital circuits has become a critical target for designers. A fundamental method for reducing the power consumption is voltage scaling which leads to a quadratic reduction in dynamic power. On the other hand, to maintain the performance of design, the threshold voltage of transistors is decreased leading to increase in the leakage current of the circuits. Also, short channel effects cause considerable increases in the leakage current of the nano-scaled MOSFET transistor. One may reduce the leakage power by reducing the subthreshold swing which may not be decreased below 60mV/decade for conventional MOSFET device structures [1]. Hence, for low-leakage power application one may replace conventional MOSFET structures with devices having smaller swings.

One of these alternative devices is Tunnel Field Effect Transistor (TFET) which is known for its steep sub-thermal subthreshold swing [1]. TFETs are P-i-N gated diodes,

operating under reverse bias condition, with a gate over the intrinsic region. They are good candidates to operate at low supply voltages ($V_{dd} < 0.3$V) while having ultra-low leakage power. The current generation mechanism in TFETs is band to band tunneling of carriers across a reversed biased PN junction [1]. Nowadays, III-V TFETs with small and direct band gap have acceptable ON-current compared to those of MOSFETs [2]. Therefore, unlike MOSFETs, reducing the (leakage) power consumption is possible for TFETs without any degradation in the performance. In [3], a mixed TFET-MOSFET 8T SRAM was proposed providing a significant improvement in the performance as well as the minimum operating voltage.

While enjoying TFET advantages in terms of leakage and power consumption, their reliability issues should also be considered and investigated. The reliability of these circuits may significantly be affected by the process variation which causes uncertainties in the (design) parameters of fabricated devices. Several studies have compared the impacts of the process variation on the performances of TFET and MOSFET devices [4,5,6]. For instance, in [4], by comparing the changes of the ON-current for a Heterojunction TFET and Silicon MOSFET, it was concluded that TFETs were more sensitive to the process variation. In [7], the influence of the process variation on the electrical parameters of III-V TFET were studied and their statistical distributions were extracted and compared to those of MOSFET devices. To increase the reliability of TFET-based circuits, in [8], a heuristic algorithm for generating hybrid TFET-MOSFET based circuits was introduced. In this algorithm, some of the TFET-based gates whose variation degraded the performance (speed) of the circuit were replaced by their MOSFET-based gates.

Radiation hardness is another important issue in designing reliable circuits. Radiation-induced single-event upset (SEU) leads to the generation of soft errors and radiation unreliability issues [9]. Furthermore, increasing the number of processing elements (as is the case for data centers) on one side and the technology scaling on the other side, make satisfying soft error immunity requirements increasingly challenging. In every generation, technology scaling roughly leads to a 30% decrease in node capacitance, 30% decrease in the supply voltage, and doubling clock frequencies. As a byproduct of these changes, the soft error rate (SER) per logic state bit increases by 8% [10]. Also, from a totally different perspective, compared to silicon, low band gap materials such as InAs, generally have low ionization energy making them more susceptible to neutron radiation which generates soft errors [11].

The investigation of the soft error phenomenon in TFETs in [11] showed that TFETs had a different soft error generation behavior than that of MOSFETs. In [12], we investigated and compared the behavior of TFETs and MOSFETs in terms of generation and propagation of the soft error. The results indicated that TFETs possessed better performance in terms of the generation of soft errors while MOSFETs were able to mask the generated current better. Inspired by this difference in behaviors, then we proposed a hybridization algorithm to generate soft error resilient MOSFET-TFET based circuits.

In this work, we propose a design approach to increase the reliability of TFET-based circuits considering the process variation and soft error phenomena. In the first step, the characteristics of III-V TFET and MOSFET devices in the presence of the process variation and particle hits are compared. In the second step, for ultra-low (static and dynamic) power applications, we suggest a hybrid TFET-MOSFET circuit design approach which minimizes the impacts of the process variation and improves the soft-

error resiliency compared to the cases where only of these device types are used. To optimize the efficacy of the approach for each application, the designer may set one of these phenomena as the one with the higher priority in the design process. Finally, the efficacy of the proposed approach is investigated by applying the method to some circuits from the ISCAS'89 benchmark package. It should be noted that the overall fabrication processes for TFETs are compatible with CMOS process [13,14], and hence, it is possible to have hybrid circuits as stated in [13,14,15]. Of course, the fabrication of TFET circuits costs more and is more complicated [15]. Finally, it should be mentioned that the proposed hybridization approach is efficient for the range of supply voltages where the performances of both TFET and MOSFET devices are similar.

The rest of paper is organized as follows. Section 2 compares the characteristics of the InAs TFET device and with those of the InAs MOSFET device. The hybridization approach realized by a proposed heuristic algorithm is discussed in Section 3. The efficacy of the proposed algorithm in increasing the reliability in the presence of soft error and process variation is evaluated in Section 4. Finally, the paper is concluded in Section 5.

2 TFET device and its characteristics
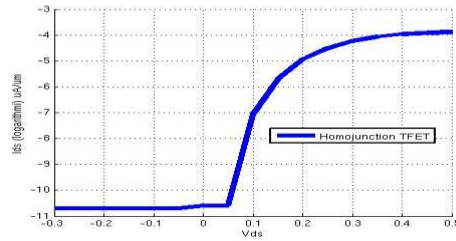
2.1 TFET device model

In this work, for obtaining an ultra-thin 22nm double-gate InAs homojunction TFET, the TCAD simulation was used. The nominal parameters of the device model which were adapted from [16], [8], and [12] are summarized in Table 1. Also, the structure and band diagram of the device are shown in Fig. 1. All the device level simulations have been performed using Silvaco ATLAS version 5.18.3.R. The activated physical models included non-local band to band tunneling, band gap narrowing, Shockley-Read-Hall model, and mobility model. The output characteristic of the Homojunction TFET (I_d-V_{ds}) is shown in Fig. 2. It should be noted that, unlike MOSFETs, TFETs are uni-directional devices because of their structural asymmetry between the source and drain [1]. The ON-current of 123µA at $V_{ds}=V_{gs}=0.5$V, leakage current of 32pA, and $I_{on}/I_{off}=3.8\times10^6$ were obtained for this TFET device.

Table 1. Nominal parameters of TFET device considered in this work.

Parameter	Nominal value
Relative Gate Dielectric Permittivity	21
Body Thickness	5 nm
Gate Oxide Thickness	2.5 nm
Source Doping	$4\times10^{19}/$ cm^3
Drain Doping	$4\times10^{17}/$cm^3
Gate Work Function	4.8 eV
Channel length	22 nm
Channel width	22 nm

(a)

P++ Source

intrinsic channel

Electron Tunneling

N+ Drain

: Off state

: On state

(b)
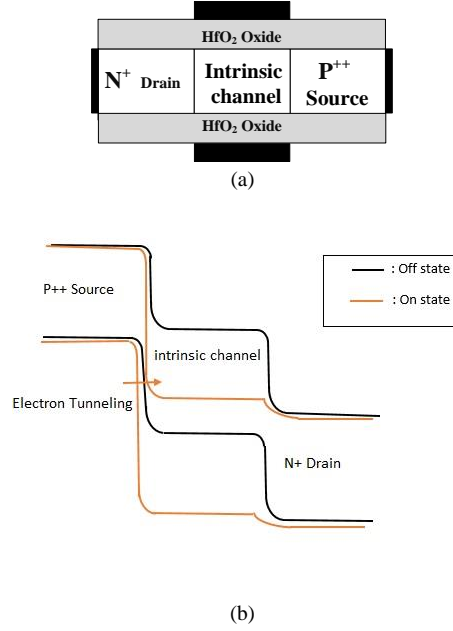
Fig. 1. TFET a) device structure and b) energy band diagram.

Fig. 2. Output characteristics of InAs TFET.

For the circuit-level simulations, Verilog-A look-up tables, which used the small sig-
nal model of Fig. 3(a), was used. Furthermore, the validity of the model was verified
by the transient output characteristics of InAs TFET inverter (see Fig 3 (b)). The con-
sidered structure of InAs MOSFET was also an ultra-thin 22nm double gate. To have a
meaningful comparison (and better hybridization during the design), the nominal pa-
rameters of the MOSFET were selected similar to those of TFETs except for the high
drain doping level (the same as that of the source) which was necessary for this struc-
ture.
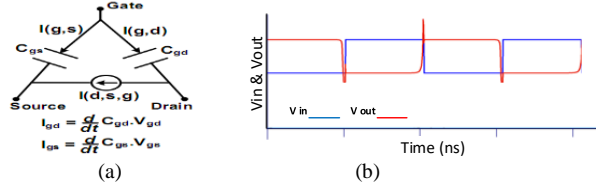
Fig. 3. a) Verilog-A small signal model and b) transient response of a TFET inverter based on the model.

2.2 Comparison of TFET and MOSFET operation

In this subsection, a comparative study on the leakage current, drive current, dynamic power consumption, sensitivity to process variation and soft error generation and propagation of both III-V MOSFET and TFET devices based on our prior works of [8] and [12] are performed.
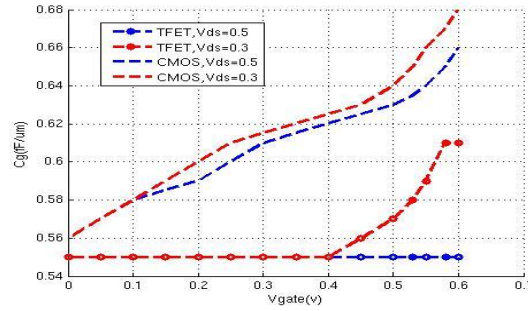
Current and capacitance comparison.

The ON-current of the III-V TFET and MOSFET device under two operating voltage levels are compared in Fig. 4 which indicate that the TFETs has lower leakage current and higher ON-current at low voltages. On the other hand, as is demonstrated in Fig. 4(b), in spite of the low leakage current of the TFET at high supply voltages, the MOSFET device has a higher ON-current which would lead to a higher performance at high supply voltages for the circuits realized by this device. Also, Fig. 5 compares TFET and MOSFET total capacitances. The comparison indicates that the gate capacitance (C_g) of the TFET is smaller than that of the MOSFET where the difference enlarges as the gate voltage is increased. The lower capacitance, which is due to the lighter drain doping of the TFETs [17], leads to a smaller gate capacitance (C_{gg}) (and hence, lower dynamic power consumption) for the TFET device.

In MOSFETs, the dominant capacitance is the gate-source capacitance (C_{gs}) while in TFETs, the gate-drain capacitance (C_{gd}) is the dominant one [17]. This would imply a larger ON-state Miller capacitance for TFETs [3], and consequently, larger induced voltage spike during the switching giving rise to increased total dynamic power consumption. Considering the capacitance and ON-current characteristics of both the TFET and the MOSFET, the supply voltage range in which the overall performance of TFET and MOSFET is close to each other, is about $0.45V < V_{dd} < 0.55V$.
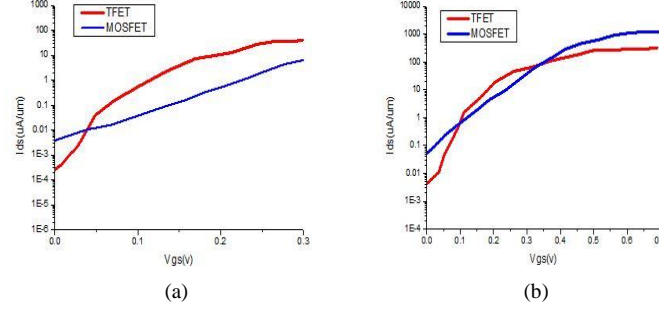
Fig. 4. Comparison of leakage current and ON-current at a) $V_{dd} = 0.3$V and b) $V_{dd} = 0.7$V.

Fig. 5. Comparison of capacitance C_g-V of the TFETs and MOSFET devices at different supply voltages.

Process variation.

As discussed earlier, compared to MOSFETs, TFETs are more prone to the process variation. In [7], we investigated the impact of the process variation on the physical parameters of InAs TFET in the presence of the process variation. The investigation was performed by utilizing the Monte-Carlo simulations where the distributions of threshold voltage and ON-current were extracted for 1000 samples. The results presented in the work showed a threshold voltage variation of about 75mV (45mV) for the 22nm InAs TFET (MOSFET) device. This implies more sensitivity to the process variation for the TFET device. It is attributed to the fact that the ON-current and subsequently the threshold voltage of the TFET device have exponential dependences on the electric field making them more susceptible to the sources of variations.

Table 2 summarizes the statistical parameters considered for the distributions of variation sources while Table 3 reports the means and standard deviations for the electrical parameters of the InAs TFET [7].

Table 2. Statistical parameters considered for the distributions of variation sources in the homojunction TFET.

Physical parameter	Mean	Standard Deviation
Gate oxide thickness	2.5nm	0.5nm
Body thickness	5nm	1nm
Gate alignment	0	3nm
Gate work function	4.8ev	0.08ev
Source doping	4e19	0.8e19
Drain doping	4e17	0.8e17
Channel length	22nm	2nm

**Table 3.** Means and standard deviations of the electrical parameters for the TFET.

Parameter	Nominal	Mean	Standard Deviation
Threshold voltage	123 mV	137 mV	75mV
ON-current	123 μA	121 μA	26.9 μA

**Soft error generation and propagation.**

Radiation induced single-event upset (the soft error) is a key challenge due to large number of computation nodes in circuits. Using low bandgap materials, scaling the supply voltage, and the reduction of capacitance of the internal nodes have made designing soft-error resilient circuits more challenging. The energetic particles, such as cosmic ray neutrons and alpha particles, are the sources of soft errors [11]. The energetic particles strike the sensitive nodes and travel through the bulk of the transistor. The creation of the minority carriers during the travel of the particles and the collection of them by the source/drain diffusion, can change the voltage value of the victim node. In other words, soft error occurs when the collected charge at a specific node is greater than the critical charge (Q_{crit}) of the node [18].

The particle hit and the change in the value of the node can be modeled by a transient current pulse [19]. In [12], we have investigated the transient current generation and soft error propagation in III-V TFETs and III-V MOSFETs, using TCAD device models and HSPICE simulations. As discussed in detail in [12], to analyze the behavior of the transistor after the ion strike, the radiation-induced transient current evaluation was performed. The generated charges, due to the particle hit, result in a transient current when the device is in the off state. ($V_{gd}=V_{dd}$, $V_{gs}=0$). The transient current generation and charge collection in fully depleted channel devices such as MOSFETs, FinFETs, and TFETs are significantly influenced by the bipolar gain effect [11]. Fig. 6 compares the generated transient current profile for the InAs TFET and the MOSFET. As the figure demonstrates, the duration and amplitude of the transient current of the TFET are about 80% and 70% smaller than those of the MOSFET. It suggests that TFET devices are more immune to the soft error generation. Here, as an example, Fig. 7 shows the output voltage spike of a MOSFET- and TFET-based FO4 inverter when a particle with a charge density of 50 fC/μm strikes the input of the inverter. The output voltage spike of the MOSFET-based inverter is up to 310mV while the voltage change for the TFET-based inverter is about 140 mV. Therefore, the generated voltage spikes in the case of the TFET-based gates are smaller compared to those of the MOSFET-based gates.
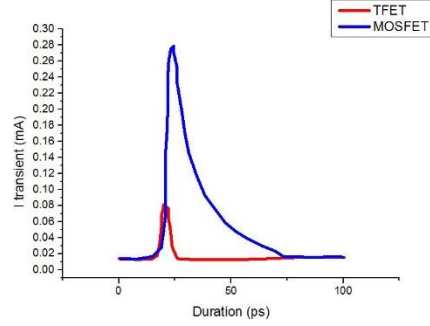
Fig. 6. Profiles of the generated transient current for the InAs TFET and MOSFET.
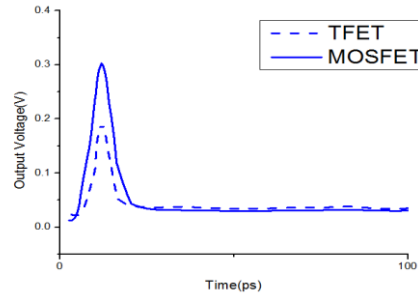
Fig. 7. Output voltage of MOSFET and TFET-based FO4 inverters after particle hit.

The generated transient current due to the particle strike induces a voltage pulse, known as a glitch, which may propagate through logic paths in the circuit. The voltage pulse may be electrically masked due to the delay of logic gates. If it is not masked, an error would happen when the generated voltage pulse either is latched by a flip flop or reaches to a primary output node of the circuit. Therefore, to conduct a complete investigation of the soft error rates in TFET- and MOSFET-based circuits, the propagation of glitches (due to the particle hits) in each type of the circuits was also considered and studied in [12]. In this work, it was concluded that TFETs propagate glitches more easily compared to MOSFETs indicating lower electrical masking for TFETs. The observed behavior is attributed to the fact that the smaller overall capacitance of TFETs compared to that of MOSFETs (see subsection 2.1). In addition, as mentioned before, at low supply voltage levels ($V_{dd} < 0.3V$), the TFET has higher ON-current compared to that of the MOSFET. This yields a higher probability for the error propagations (less masking) by the TFET device (the TFET-based gate). Fig. 8 shows the voltage spikes at the output nodes of two inverter chains when a particle with a charge density of 50 fC/μm hits the input of the chain. As the figures demonstrate, the amplitude of the voltage spike at the output of the chain in the case of MOSFET-based implementation is smaller than that of the TFET-based implementation showing a better masking for the MOSFET one.
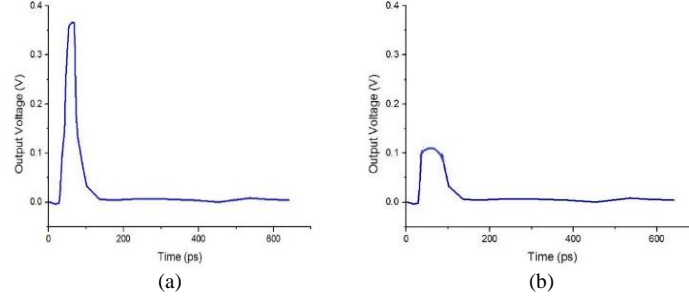
Fig. 8. Output voltage of the chains of three a) TFET-based and b) MOSFET-based inverters after the particle hit the input of chain.

As the conclusion of this part, we showed that the TFET device exhibited a better characteristic in terms of the generation of the transient current due to the particle hit while the MOSFET device revealed a better characteristic for the electrical masking of the transient current due to the particle hit [12].

3   Hybrid TFET-MOSFET circuits

3.1   Why hybridization?

As mentioned previously, while the TFET leakage power and (dynamic) energy consumption are smaller than those of the MOSFET, the relation between the speeds (and delays) of the TFET and MOSFET circuits depend on the operating voltage. Also, the process variation impacts the electrical parameters of the TFET more compared to the MOSFET. Hence, the probability of timing violation in TFET-based circuits is higher. Furthermore, the generated transient current is weaker in TFETs despite the fact that MOSFETs have better performance in masking these errors.

As mentioned before, to take advantage of both TFETs and MOSFETs superior features, robust ultra-low power circuits were proposed in [8] and [12]. To increase the reliability of TFET-based circuits in the presence of the process variation, a heuristic algorithm was proposed in [8] which replaced the TFET-based gates in the potential critical paths with their corresponding MOSFET-based gates. In the proposed approach, the hybridization process (gate replacement) started from the initial stages of the circuit. The results showed about 50% increase, on average, in the reliability of hybrid TFET-MOSFET based gates compared to the pure TFET-based gates when applied to ISCAS'85 and ISCAS'89 benchmarks.

Another hybridization algorithm, which was proposed in [12], focused on decreasing the soft error rate of TFET-based circuits, again, by replacing some of the TFET gates by their corresponding MOSFET ones. The TFET-based gates are superior to MOSFET-based ones in terms of the error generation, while the latter mask the error more efficiently. Thus, to have a soft-error resilient design, one should have the TFET-based gates in the generation path of the transient (error) current and the MOSFET-based ones in the propagation path of the transient (error) voltage. Based on these features, in the proposed algorithm of [12], first, the sensitive internal nodes were chosen.

The sensitive nodes considered to be the nodes with small capacitance and high probability of generating the voltage spike. Then, for each chosen sensitive node, the first gate of each path starting from the sensitive node, was considered to be implemented by TFETs. This resulted in generating smaller voltage pulses due to particle hits. However, the gates in the second and third levels were considered to be implemented by MOSFETs to electrically mask the generated voltage pulses. Furthermore, a hybrid soft-error resilient flip-flop was proposed in [12]. Applying the proposed algorithms to the circuits from the ISCAS'89 benchmark package as well as utilizing the hybrid flip-flop in these circuits led to, on average, 80% decrease in the soft-error rate compared to those of the pure TFET-based designs.

These prior works showed that the hybridization resulted in improvements in the timing yield as well as the soft error immunity. While each of these hybridization approaches improved the performance of the circuit against the impact of one of these undesired phenomena, in this work, we focus on enhancing the circuit operation in the simultaneous presences of the process variation and soft error. In the next subsection, the proposed hybridization algorithm is described in detail.

3.2   Proposed Heuristic Hybridization Algorithm

The flow of the proposed algorithm may be divided into three major parts. In the first part of the algorithm, which is shown in Fig. 9, the operating supply voltage level, potential critical paths, and sensitive nodes to the soft error are determined. In the first step of this part (❶), in order to avoid the degradation of the speed of the circuits after the hybridization, the supply voltage level which leads to almost the same delays for both the TFET- and MOSFET-based implementations of the input design is determined. The delays of both pure TFET and MOSFET circuits should be smaller than a predefined delay (*i.e.*, D_{const}). This is an iterative process which is performed by using HSPICE simulations under different supply voltage levels. It starts by the parameter V_{start} as the initial operating voltage level and continues by increasing the voltage by V_{step} at the end of each iteration. In each iteration, the delays of both TFET- and MOSFET-based circuits are compared. If the delays have an acceptable delay difference with both delays smaller than D_{const}, this process is terminated. Otherwise, the process is repeated by increasing the supply voltage level. In this work, we considered the delay difference of smaller or equal than 10% of the delay of MOSFET-based circuit as the acceptable delay difference. The reason for considering the 10% delay difference as the acceptable value was to lower the effort for finding the supply voltage for the similar performances for all the implementations.

Based on the ON-current values which were given in Section 2, in this work, we consider 0.4V as V_{start}. Also, our study showed that the selected supply voltage levels for different circuits did not exceed 0.55V. It is worth mentioning that if D_{const} is too small, the process would not converge to a supply voltage level, and hence, D_{const} should be increased in these cases. Obviously, the lower supply voltage is translated to lower power consumption and, hence, the search process starts from the lowest supply voltage.

After determining the supply voltage level, the set of potential critical paths (*i.e.*, S_{PCP}) of the TFET-based circuit is determined by using static timing analysis (STA) (❷). In

this work, the paths which have delays larger than 80% of the longest path, are considered as the potential critical paths. For performing the hybridization, we propose to start from TFET-based implementation of the design while all the flip-flops are implemented by the proposed hybrid approach of [12]. Hence, after determining the supply voltage level and critical paths, the capacitances of the internal nodes are extracted and a collection of sensitive internal nodes are chosen (*i.e.*, S_{SIN}) (❸). As mentioned previously, the sensitive nodes are the nodes with small capacitances where the probability of generating the voltage spike due to the particles hit on these nodes is high. Here, a node whose capacitance is less than or equal to 1.2 times of the smallest internal node capacitance of the circuit is specified as the sensitive node. In the proposed flow, the objective is both to increase the timing yield and decrease the soft error rate. The designer, in this step, based on the priority specified by the designer, one the two hybridization paths is selected (❹). If the priority is given to the soft error-resiliency (process variation mitigation), the next steps of the algorithm put more emphasis on reducing the impact of the soft error (process variation) while attempting to decrease the impact of the process variation (soft error) with a lower priority effort. Next, the details of the algorithm in the cases of process variation mitigation and soft error resiliency priorities are explained.
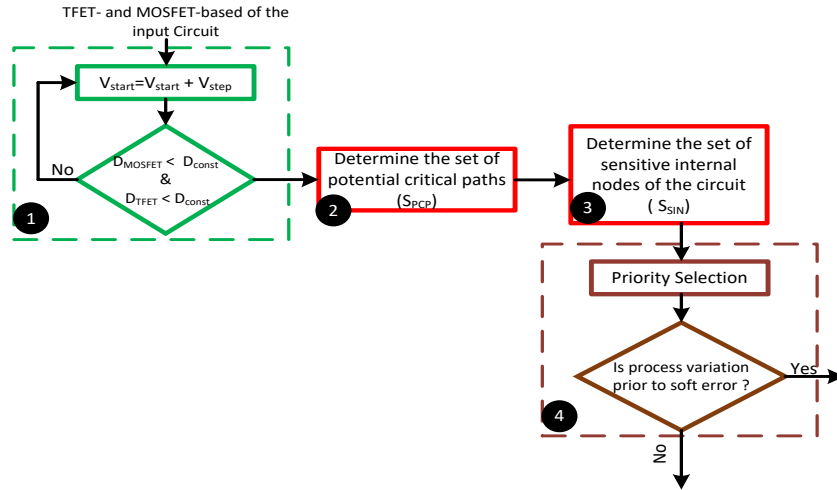
Fig. 9. First part of the proposed algorithm which is common between the two hybridization paths.

Priority on process variation mitigation.

Fig. 10 shows the rest of the proposed algorithm for the case where the process variation mitigation is selected as the main priority of the hybridization. For this case, similar to [8], the hybridization process for each path starts from the first gate of the path owing to the fact that the delay variation at the beginning stages of TFET-based designs is larger. By starting the replacement process from the beginning gates, one mitigate the delay variation of the path more by replacing smaller numbers of gates [8].

In the first step of the proposed flow (❶), for each potential critical path, the delay distribution of the MOSFET-based implementation is extracted (*i.e.,* $(\sigma/\mu)_{\text{MOSFET}}$). The delay distribution of the MOSFET-based implementation is used as a reference point for the next phase of the algorithm. The process of extracting the delay distribution may be performed by exploiting either statistical static timing analysis (SSTA) or Monte-Carlo simulation. The former approach is fast and inaccurate while the latter one is accurate and slow. In this work, we have used Monte-Carlo simulations to extract the delay distributions of the potential critical paths.

For each potential critical path, after determining the delay distribution of the MOSFET-based implementation, the hybridization process for this path in the TFET-based implantation circuit is performed (❷). This process is an iterative process, which starts from the first gate of the path and continues to the last gate of the path. In each iteration, first, the delay variation of the path is extracted, and if the delay variation of the path ($(\sigma/\mu)_{\text{hybrid}}$) becomes smaller than the $\alpha \times (\sigma/\mu)_{\text{MOSFET}}$, the process for this path will be terminated. Otherwise, the TFET-based gate is replaced by the MOSFET-based gate, and the process is repeated for the next gate. The parameter α, which is a predefined coefficient specified by the designer, determines the expected delay variation of the hybrid TFET-MOSFET-based design compared to that of the MOSFET-based design. It should be noted that, for each new path, the hybridization process does not reconsider the gates which have been replaced by MOSFET-based ones in the previous iterations. This case may occur when some potential critical paths have a shared gate.

After applying the proposed method for increasing the timing yield of the circuit, we take an approach to decrease the soft error impact on the reliability of circuits (❸). In this step, the sensitive internal nodes are chosen one by one where for each chosen sensitive node, all the paths which start from this node are extracted. Due to the better behavior of TFETs in generating transient currents, this type of gates are preferred. If, however, these gates are located in the critical paths, they are not replaced by TFETs if they are MOSFET-based gates as dictated by the previous hybridization part. If the gates are not in the critical paths, the third step of hybridization starts. For each extracted path, the first gate of the path is considered to be implemented by TFETs. This leads to generating a smaller voltage pulse due to the particle hit. The gates in the second and third levels are considered to be implemented by MOSFETs to electrically mask the generated voltage pulse. Our results show that one MOSFET-based gate is not able to fully mask the generated voltage pulse, while with a high probability, two consecutive MOSFET-based gates mask more effectively the generated pulse [12].

Next, we compare the soft error rates of the path under three different implementations of TFET-based, MOSFET-based, and hybrid TFET-MOSFET-based. If the error rate of the hybrid TFET-MOSFET implementation is smaller than the other two implementations, the hybridization for this path is terminated while, if the error rate of the hybrid TFET-MOSFET path is larger than that of the other implementations, the first gate after the last MOSFET-based gate (which is initially TFET-based) is considered to be implemented by a MOSFET one. This process is carried out till either the soft error rate of hybrid path reaches to a value smaller than the soft error rates of the two other implementations or there are no more gates in the path for the replacement. When the process of the hybridization for all the extracted paths of a sensitive node is terminated, the algorithm chooses another sensitive node and applies the above replacement procedure to the gates of its paths.

Note that replacing a TFET-gate by a MOSFET-gate may result in a capacitance increase of the internal nodes of the circuit connected to the inputs of this gate. Hence, after finalizing the hybridization of all the paths of a sensitive node, all the capacitances of the internal nodes of these paths are extracted. Now, if the capacitance of a node which belongs to the sensitive list increases to a value higher than the considered threshold value for the sensitive nodes, this node is removed from the sensitive nodes list.
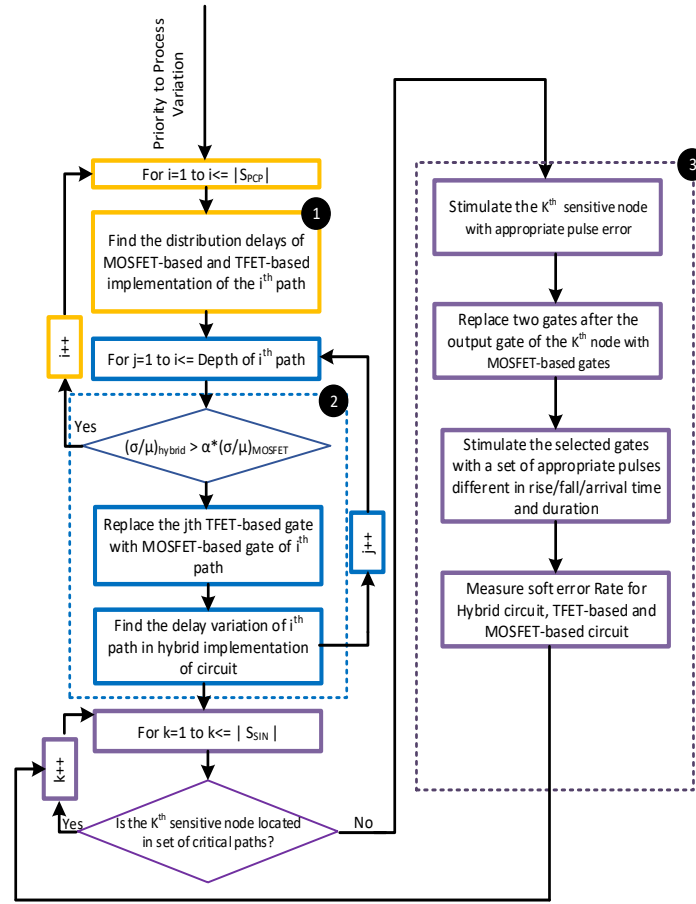

Fig. 10. Second part (priority on process variation mitigation) of the proposed algorithm.

Priority on decreasing the soft error rate.

Third part of the algorithm deals with the case that the priority is on decreasing the soft error rate. The flow of the this part of the algorithm is depicted in Fig. 11. The overall flow for the hybridization technique in this part is almost similar to the one described in the previous subsection. For this case, first, the sensitive nodes are extracted where for any of the sensitive nodes, all the paths starting from the sensitive

nodes are chosen. To have a soft-error resilient design, the first stage of each path is implemented in TFETs while two latter stages are implemented in MOSFETs due to the better error masking of MOSFETs (❶). Next, for each of the potential critical paths, the delay distribution of MOSFET-based and TFET-based designs are determine (❷). Finally, the hybridization technique is performed to increase the reliability of design (❸). The overall approach is as the one presented in the second step of the algorithm. In this case, however, if the gates that are located in the critical paths are the gates which are set to be implemented in TFETs due to transient current generation, they will remain unchanged and the hybridization is performed for the next step of the design.
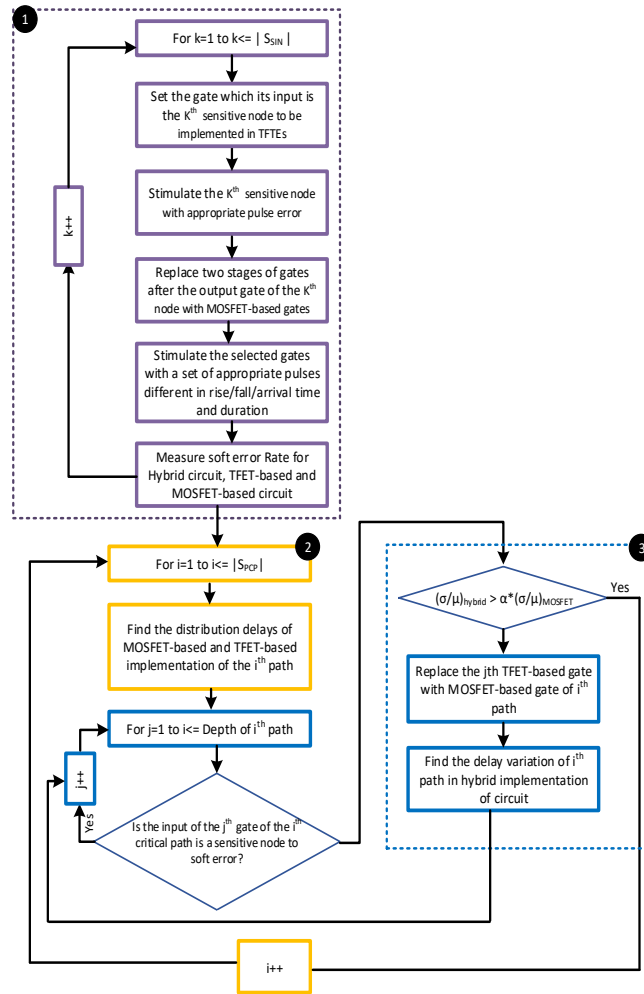

Fig. 11. Third part (priority on decreasing the soft error) of the proposed algorithm.

Now, in the following section, the efficiency of the proposed hybridization algorithm on increasing the reliability is evaluated for the two cases of priority with process variation mitigation and priority with soft error rate reduction. Also, the power consumptions for these circuit implementations is discussed.

4   Results and discussion

4.1   Simulation Framework

In this study, the results of applying the proposed design approach to some sequential circuits from ISCAS'89 benchmark package are discussed. All the simulations were performed by utilizing the HSPICE tool. As mentioned before, we have used Verilog-A models of the 22nm double gate InAs TFET and 22nm InAs MOSFETs during the HSPICE simulations. To perform the simulations, first, all of the considered circuits were synthesized to a gate-level netlists using Synopsys Design Compiler. In this work, without loss of generality, only Inverter, and 2-input NAND, NOR, AND, OR, XOR and XNOR gates were considered as the cells of the technology library. After extracting the gate-level netlist, the HSPICE netlist of the circuits were generated by using an in-house tool. In addition, the potential critical paths of the benchmarks were obtained using an in-house STA tool. It should be stated that the master-slave flip-flops of the selected benchmarks were replaced by the proposed hybrid TFET-MOSFET flip-flop of [12], to provide a more soft-error resilient design. Furthermore, the proposed heuristic hybridization algorithm was implemented using Python language. Finally, each of the studied circuits was implemented in three forms of MOSFET-based circuit, TFET-based circuit, and Hybrid TFET-MOSFET-based circuit. As mentioned before, to keep the overall performance of the circuit almost constant after the hybridization, the operation voltage was determined by the algorithm such that both TFET-based gates and MOSFET-based gates had about the same delays.

The particle hit in each critical node was modeled by injecting voltage pulses. The injected voltage pulses, which were totally 60, were different in rise time, fall time, arrival time compared to the edge of the clock, duration, and amplitude. The ranges of these parameters utilized in this work are given in Table 4. In the table, V_{error} refers to the nominal amplitude of the generated error for TFET and MOSFET transistors. During the simulations, error pulses with larger amplitudes were applied to MOSFET.

Table 4. The ranges of the values used for generating error injection voltage pulses

Parameter	Range of Values
Rise time	10ps to 100ps
Fall time	10ps to 100ps
Arrival time compared to edge of the clock	-100ps to +100ps
Duration	10ps to 300ps
Amplitude	$V_{error} \pm 0.1V$

### 4.2 Comparison of different implementation efficiencies

In this section, the efficacy of the proposed hybridization algorithm is evaluated. The normalized leakage power, energy consumption, delay variation, and soft error rate of the hybrid benchmarks are measured and compared to MOSFET-based and TFET-based designs. The normalized values of these parameters for each implementation of each benchmark circuit are shown in Fig. 12. In this figure, the values of the leakage power and energy consumption are normalized to the leakage power and energy consumption of the MOSFET-based design while the values of the delay variation and soft error rate are normalized to those of the TFET-based design.

As was mentioned in the previous section, the algorithm allows the designers to specify either the soft error or process variation mitigation as the higher priority. Here, we present the results for the application of the algorithm to each benchmark, considering both cases. As the results indicate, for both cases, the delay variation mitigation and soft error rate reduction of the hybrid design are improved compared to those of the pure TFET-based design. Also, the delay variation (soft error rate) of circuits decrease more in the case that the process variation mitigation (soft error rate reduction) has the higher priority. In addition, the proposed design approach decreases the leakage power and energy consumption compared to those of the MOSFET-based design for both cases. It should be emphasized that the pure TFET-based design offers lower leakage power and energy consumption while pure MOSFET-based design provides smaller delay variation. The hybrid design has lower delay variation compared to that of the pure TFET design and smaller leakage power and energy consumption compared to those of the MOSFET design.

Now, we discuss these results in more detail. In the case of S838 (S713) circuit, the leakage power (energy consumption) decreases about 75% (67%) compared to the MOSFET-based design while, compared to the TFET-based circuits, the leakage power (energy consumption) only increases about 14% (15%). For the delay variation, the highest reduction belongs to the S838 benchmark with the delay variation of about 66% when process variation mitigation has the higher priority. When the priority is given to soft error resiliency of the design, the maximum reduction in the delay variation is about 58% belonging to S344 circuit. Considering the results for the soft error rates, the maximum reduction of 87% is for the S344 circuit in the case of the soft error reduction priority and the maximum reduction of 73% for the S344 circuit in the case where the priority is for the process variation mitigation. The study shows that, the proposed hybrid approach leads to, on average, 64% (48%) leakage power (energy consumption) reduction compared to the case of the MOSFET-based design when the process variation has the higher priority. Also, compared to the TFET-based design, it provides, on average, 52% delay variation reduction and 71% soft error rate reduction. On the other hand, when the priority is given to the soft error issue, the approach results in, on average, 67% (50%) leakage power (energy consumption) reduction compared to that of the MOSFET-based design as well as 42% (80%) decrease in the delay variation (soft error rate) decrease compared to that of the TFET-based circuit.

The results for the delay variation and soft error rate of the S27 and S344 circuits are the same in both priority cases of the proposed algorithm. It originates from the fact that, in these circuits, none of the sensitive nodes is located in the critical path. Therefore, the critical paths may be completely implemented using MOSFET-based gates

wherever necessary. Similarly, we can keep TFET-based gates whenever shorter and smaller transient current are preferred. Hence, a complete hybridization is performed to reduce both delay variation and soft error rate.
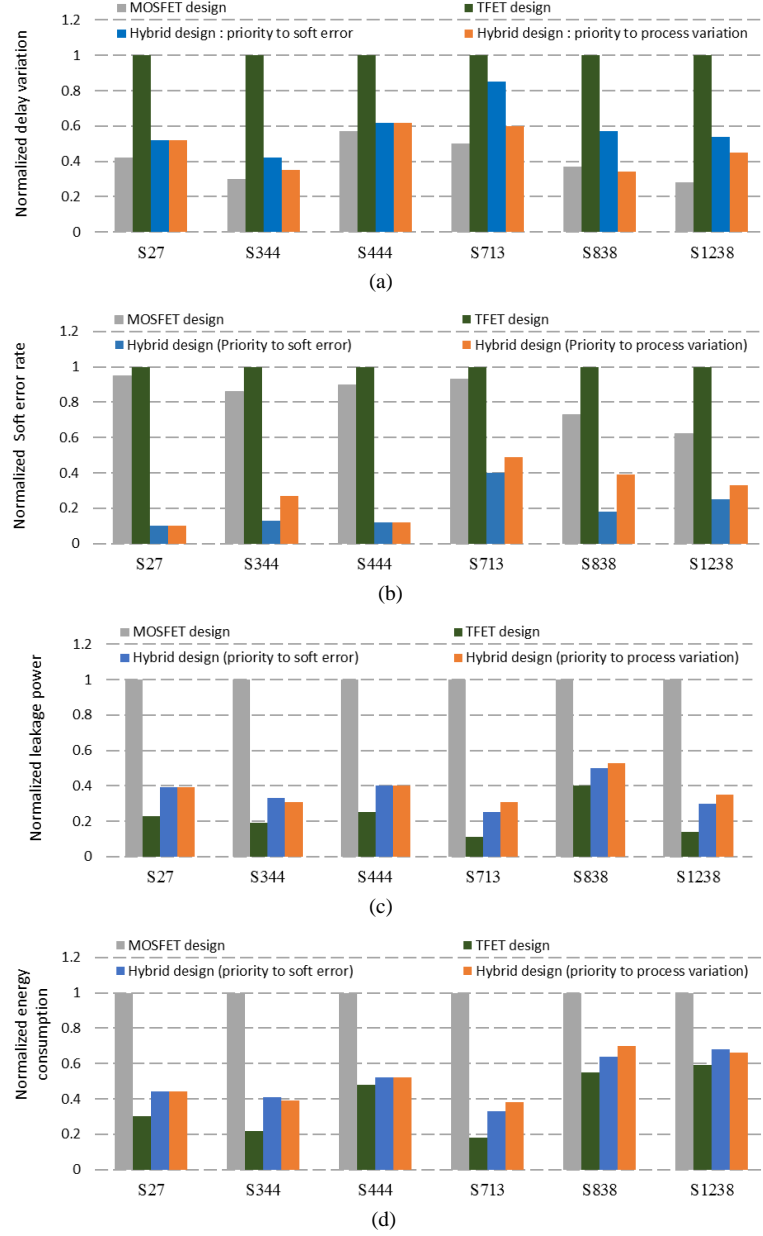
Fig. 12. Normalized a) delay variation, b) soft error rate, c) leakage, and d) energy, for some circuits from ISCAS89 benchmark package.

Finally, to illustrate the significance of each of the defined priority cases in the algorithm, we define a parameter which is the ratio of the number of sensitive nodes located in the set of potential critical paths of the circuit to the total number of sensitive nodes. The ratio is called Sensitive Nodes in Critical Paths (SNCP). The larger the SNCP is, the more sensitive nodes are located in the critical paths. Hence, when the priority is given to the soft error rate reduction, the delay variation of the circuit becomes larger. On the other hand, if the priority is given to the process variation mitigation, the circuit with larger SNCP, will have greater soft error rate. Fig. 13 depicts the SNCPs for different benchmarks. Interestingly, the S27 and S344 circuits have SNCP values of zero, making leading to the same results for both priority cases.
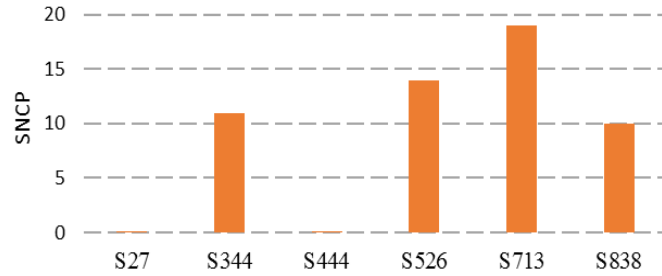
Fig. 13. Parameter SNCPs (Sensitive Nodes in Critical Paths) for different benchmarks.

5   Conclusion

In this paper, a hybrid TFET-MOSFET design was proposed to decrease the probability of timing violation and soft error rate in TFET-based designs. The hybridization method was inspired by the features of TFET and MOSFET devices. First, compared to MOSFET, the process variation impact was more on the TFET characteristics. Second, while the transient current, generated by a particle hit, was shorter and smaller for TFETs, MOSFETs had better electrical masking of these pulses. In this work, first, a III-V TFET model was selected and the impact of the process variation on its output electrical characteristic as well as soft error generation and propagation were investigated. Next, considering the operation and characteristics of both TFET and MOSFET devices, a heuristic algorithm was proposed for the TFET-MOSFET hybridization design. Finally, the proposed algorithm was applied to some sequential circuits of the ISCAS'89 benchmark package. The results showed that the delay variation of the TFET-MOSFET-based circuits, on average, would decrease about 52%, compared to that of the TFET-based circuits, if the priority were given to the process variation mitigation. The decrease in the variation was about 42%, on average, for the case with the soft error rate reduction priority. On the other hand, the soft error rate of the TFET-MOSFET-based circuits decreased about 80%, on average, when the priority was given to the soft error issue. The reduction of soft error rate was about 72%, on average, if the priority was given to the process variation mitigation. These results suggested that one TFET-MOSFET hybridization technique may be employed effective to improve the

yield and soft error immunity characteristics of ultra-lower power circuits based on pure TFET-based design circuits.

6   References

[1]   Mukundrajan, R., Cotter, M., Saripalli, V., Irwin, M., Datta, S., Narayanan, V.: Ultra low power circuit design using Tunnel FETs. In: IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 153-158. IEEE press, MA(2012)

[2]   Kim, M. S., Liu, H., Swaminathan K., Li, Xi., Datta, S., Narayanan, V.: Enabling Power-Efficient Designs with III-V Tunnel FETs. In: IEEE Compound Semiconductor Integrated Circuit Symposium (CSICs), pp. 1-4. IEEE press, Califoria(2014)

[3]   Chen, Y.-N. , Fan, M.-L. ,. Hu, V.-H, Su, P., Chuang, C.-T.: Evaluation of Stability, Performance of Ultra-Low Voltage MOSFET, TFET, and Mixed TFET-MOSFET SRAM Cell With Write-Assist Circuits. J. Emerging and Selected Topics in Circuits and Systems. 4, 389-399 (2014).

[4]   Migita, S. , Matsukawa, T. , Mori, T. , Fukuda, K. , Morita, Y. , Mizubayashi, W.: Variation behavior of tunnel-FETs originated from dopant concentration at source region and channel edge configuration. In: 44th European Solid State Device Research Conference (ESSDERC), pp. 278-281. IEEE press, Venice (2014).

[5]   Zhang, L. , Chan, M., He, F.: The impact of device parameter variation on double gate tunneling FET and double gate MOSFET. In: IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC), pp. 1-4. IEEE press, Hong Kong (2010)

[6]   Damrongplasit, N. , Shin, C. , Kim, S. H. , Vega, R. A., Liu, T.-J. K.: Study of random dopant fluctuation effects in germanium-source tunnel FETs. J. Electron Devices. 58, 3541-3548 (2011)

[7]   Hemmat, M., Kamal, M., Afzali-Kusha, A., Pedram, M.: Study on the impact of device parameter variations on performance of III-V homojunction and heterojunction tunnel FETs. J. Solid State Electronics. 124, 46-53 (2016)

[8]   Hemmat, M., Kamal, M., Afzali-Kusha, A., Pedram, M.: Hybrid TFET-MOSFET circuits: An approach to design reliable ultra-low power circuits in the presence of process variation. In: IEEE International conference on Very Large Scale Integration (VLSI-SoC),pp. 1-6. IEEE press,Tallinn (2016)

[9]   Dhillon, Y. S., Diril, A. U. , Chatterjee, A. : Soft-error tolerance analysis and optimization of nanometer circuits. In: IEEE International conference on Design, Automation, and Test in Europe, pp. 389-400. Springer, GA (2008)

[10]   Liu, H. , Cotter, M. , Datta, S. , Narayanan, V. : Technology assessment of Si and III-V FinFETs and III-V tunnel FETs from soft error rate perspective. In: IEEE International Electron Devices Meeting (IEDM), pp. 25.5. 1-25.5. 4. IEEE press, California (2012)

[11]   Datta, S., Liu, H., Narayanan, V.: Tunnel FET technology:A reliability perspective. J. Microelectronics Reliability. 54, 861-874 (2014)

[12]   Hemmat, M., Kamal, M., Afzali-Kusha, A., Pedram, M. : Hybrid TFET-MOSFET circuit: A solution to design soft-error resilient ultra-low power digital circuit. J. Integration, the VLSI journal. 57, 11-19. (2017)

[13]   Tura A. : Novel Vertical Tunnel Transistors for Continued Voltage Scaling. Ph.D. dissertation, Univ. of California , Los Angeles (2010)

[14]   Chen, Y.-N. , Fan, M.-L. , Hu, V.-H. , Su, P. , Chuang, C.-T. : Evaluation of Stability, Performance of Ultra-Low Voltage MOSFET, TFET, and Mixed TFET-MOSFET SRAM Cell With Write-Assist Circuits. J. Emerging and Selected Topics in Circuits and Systems. 4, 389-399 (2014)

[15]   Mishra, A., Jha, K. K., Pattanaik, M. : Parameter variation aware hybrid TFET-CMOS based power gating technique with a temperature variation tolerant sleep mode. J. Microelectronics. 45. 1515-1521. (2014)

[16]   Liu, H., Datta, S.: III-V Tunnel FET model manual. The Pennsylvania state university (2015)

[17]   Cotter, M., Liu, H., Datta, S., Narayanan, V.: Evaluation of tunnel FET-based flip-flop designs for low power, high performance applications. In: 14th international symposium on Quality electronic design (ISQED), pp. 430-437. IEEE press, California (2013)

[18]   Miskov-Zivanov N. , Marculescu, D.: Modeling and optimization for soft-error reliability of sequential circuits. J. Computer-Aided Design of Integrated Circuits and Systems. 27, 803-816 (2008)

[19]   Lin, S. , Kim, Y.-B., Lombardi, F.: Soft-error hardening designs of nanoscale CMOS latches. In: 27th IEEE Symposium on VLSI Test, pp. 41-46. IEEE press, Washington (2009)