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Oxide TFTs on Flexible Substrates for Designing and Fabricating Analog-to-Digital Converters

Ana Correia^{1,2}, João Goes¹ and Pedro Barquinha²

¹ CTS/UNINOVA, Departamento de Engenharia Electrotécnica, Faculdade de Ciências e Tecnologia, Universidade NOVA de Lisboa, Campus da Caparica, 2829-516 Caparica, Portugal

² I3N/CENIMAT, Departamento de Ciência dos Materiais, Faculdade de Ciências e Tecnologia, Universidade NOVA de Lisboa and CEMOP/UNINOVA, Campus da Caparica, 2829-516 Caparica, Portugal
a.correia@campus.fct.unl.pt, jg@uninova.pt, pmcb@fct.unl.pt

Abstract. Thin-film transistors (TFTs) employing oxide semiconductors have recently emerged in electronics, offering excellent performance and stability, low processing temperature and large area processing, being indium-gallium-zinc oxide (IGZO) the most popular amorphous oxide semiconductor. In this work it is shown how IGZO TFTs can be integrated with multilayer high- κ dielectrics to obtain low operating voltages, both on glass and flexible PEN substrates. Then, the electrical properties extracted from these devices are used to design and simulate a 2nd-order Sigma-Delta ($\Sigma\Delta$) analog-to-digital converter (ADC), showing superior performance (e.g. SNDR \approx 57 dB, and DR \approx 65 dB) over ADCs using competing thin-film technologies.

Keywords: Amorphous oxide semiconductors, IGZO TFTs, circuit integration, ADCs, $\Sigma\Delta$ modulator.

1 TFTs for Large-Area Electronics: A Materials Perspective

Displays are deeply incorporated in our daily lives in mobile phones, TVs, monitors, among others. The key electronic elements of these displays are thin-film transistors (TFTs) responsible for switching each pixel on and off. A TFT is a particular case of a field-effect transistor (FET) based on thin-film technologies, presenting a semiconductor located between drain and source electrodes and the dielectric layer placed between gate electrode and the semiconductor. Using these three terminals (drain, source and gate), the principle behind this device is to control the current between drain and source electrodes (I_{DS}) through the gate-source potential (V_{GS}) [1].

The first conceptual patents on TFTs were reported in 1930, however these devices only acquired a high relevance in the 70s, with the advances on flat-panel displays, specially with the appearance of active matrix liquid-crystal displays (AMLCDs). Hydrogenated amorphous silicon (a-Si:H) soon started to be the preferred choice for semiconductor owing to its amorphous structure perfectly suitable for large area fabrication. Still, its low field-effect mobility ($\mu_{FE} < 1 \text{ cm}^2/\text{Vs}$) was not compatible

either with the fabrication of the peripheral drivers of the displays or for other circuits operating in the MHz range. Poly-Si was introduced to deal with this limitation, enabling $\mu_{FE} > 100 \text{ cm}^2/\text{Vs}$, but at the cost of larger processing temperatures and a polycrystalline structure, hindering low cost and uniform fabrication in large areas. On the other hand, organic semiconductor based TFTs were also introduced in the late 80s, as the ultimate technology, when low-cost and mechanical flexibility are major requirements. However, their electrical performance was (and is) comparable to a-Si:H TFTs and degradation under normal environmental conditions is a major concern.

The new millennium set the stage for a new transistor technology, able to fulfil the needs of flexible, low cost but nonetheless fast electronics. Oxide semiconductor TFTs are such technology, offering excellent uniformity in large areas using temperatures below 150°C and μ_{FE} exceeding $10 \text{ cm}^2/\text{Vs}$. In addition, most oxides have bandgaps (E_G) above 3 eV, turning them transparent materials in the visible spectrum, enabling exciting concepts such as fully transparent and flexible devices [2]. Even if some initial oxide TFTs were reported in the 60s, the most relevant works showing the potential of such technology started in 2002 with polycrystalline ZnO TFTs [3–6]. Despite the encouraging results obtained using ZnO, rapidly amorphous multicomponent materials started to be used, specially indium gallium zinc oxide (IGZO). In fact, in these amorphous oxides a “continuous path” created by spherical isotropic *ns* orbitals of the metallic cations, when the radii of these orbitals is larger than the distance between cations, allows obtaining excellent μ_{FE} even in amorphous structures [7]. Although IGZO is the most widely used amorphous oxide semiconductor (AOS), some additional combinations have been considered, as indium-free alternatives such as zinc-tin oxide (ZTO).

Despite the semiconductor used in a TFT, the dielectric choice critically affects the device performance and stability. High- κ dielectrics have been used instead of traditional SiO_2 due to different reasons. When low temperature deposition processes are used, semiconductors and their interfaces are more prone to have large defect density and poor compactness. Hence, the large capacitance per unit area of high- κ dielectrics compensates this, by inducing a larger charge density per unit voltage. This also allows for low-voltage operation: as will be seen in this work, high- κ results in less than half of the operation voltage (seen by transconductance saturation) compared to thermal SiO_2 with similar thickness. Furthermore, the larger film thickness (without compromising a good overall capacitance) enabled by high- κ dielectrics compensates the more degraded dielectric film properties fabricated at low temperatures, avoiding for instance quantum tunnelling effects. Additionally, selecting high- κ materials with an amorphous structure typically results in smoother films and, consequently, in improved interfaces with amorphous semiconductors, while the lack of grain boundaries of amorphous structures decreases the gate leakage current (I_G). However, most of the high- κ dielectrics have lower E_G than lower- κ materials as SiO_2 , which based on band alignment considerations can be problematic to obtain low I_G . Hence, multicomponent dielectrics based on combinations of materials with high- κ and high- E_G , such as Ta_2O_5 and SiO_2 , respectively, has been studied in different configurations, taking advantage of structural and electrical properties of both materials [8].

2 Relationship to Cyber-Physical Systems: From Oxide TFTs to a Complete System-on-Foil

The current advances in oxide TFTs are changing and expanding the display market, enabling higher refresh rate combined with ultra-definition and stimulating new approaches such as curved or transparent displays. The big players in the multi-billion dollar display industry are naturally all aware of this TFT technology, with an increasing number of prototypes and even commercial products being available from companies as Samsung and LG. One of the most relevant examples is the line of curved OLED TVs by LG, making use of oxide TFT backplanes.

Despite all this activity in taking oxide TFTs to displays, efforts have also been done to take full advantage of oxide TFTs and integrate them in other electronic circuits and systems. In fact, good uniformity over large area, excellent electrical performance and stability, low production costs and the flexible or even recyclable concepts encourage their integration in full system-on-foil concepts, expanding their functionality and their applicability. To the author's best knowledge, the first circuits using oxide TFTs appeared in 2006, in which inverters and a five-stage ring oscillator (RO) have been reported using indium-gallium oxide (IGO) TFTs. Regarding inverters, a peak gain magnitude close to 1.5 was measured and a maximum oscillation frequency of 9.5 kHz has been experimentally demonstrated [9]. Several RO performance improvements have been achieved by decreasing the propagation delay and, therefore, allowing to increase the maximum oscillation frequency and the number of cascaded stages [10, 11]. Shifter registers, current mirrors and a digital-to-analog converter (DAC) were also produced using oxide TFTs. Regarding DAC, which is already a circuit realization with a considerable level of complexity, encouraging results were achieved using IGZO TFTs, showing a spurious-free dynamic range (SFDR) above 30 dB up to 300 kHz and a sampling rate of 1 MS/s [12]. It is also relevant to notice the relatively recent developments of using TFTs in applications spanning from near-field communications (NFC) to radio-frequency identification (RFID) tags. In 2011, the first RFID chip was produced using IGZO TFTs, showing a small power dissipation (20 μ W) making it suitable for short-range wireless operation [13]. In 2015, a fully flexible NFC tag also using IGZO TFTs has been fabricated, exhibiting excellent performance, as a maximum data rate close to 72 kbits/s [14]. These last examples intensify the potential of using oxide TFTs for an entire system-on-foil concept where, besides performance and processability of electronic devices in low cost and flexible substrates, multifunctionality of the platform using only one semiconductor technology is a paramount advantage in terms of reliability and cost of the complete system.

The referred system-on-foil concept plays a relevant role nowadays in the global cyber-physical systems (CPS) approach, which combines computation and physical processes networking and it is transversal to multiple fields of knowledge, involving areas such as healthcare, energy or consumer appliances. In fact, the excellent performance and stability of oxide technologies are key enablers to develop innovative, more efficient and high frequency systems, improving strongly the communication in complex systems.

3 Oxide TFTs Produced at FCT-NOVA

Oxide TFTs have been studied using different approaches in order to optimize and enhance TFT performance, and reducing at the same time the involved fabrication costs. For that end different materials, structures and processes, such as the usage of organic insulators, nanowire structures and solution processes, respectively, have been studied in different research groups worldwide, including CENIMAT and CEMOP at FCT-NOVA. This section summarizes a small part of these developments, which were then used as the basis to design the ADC case study presented in section 4. In this case, since complex circuit design demands for good performance and stable devices, sputtered IGZO was selected as the semiconductor, given that it is the most mature process/material available in-house. IGZO was then coupled with different sputtered high- κ dielectrics based on Ta_2O_5 and SiO_2 , evaluating the effect of the dielectric on important device parameters such as μ_{FE} , turn-on voltage (V_{on}) and I_{G} .

3.1 Devices Fabrication and Characterization

IGZO TFTs were produced on Corning Eagle glass and on flexible Polyethylene Naphthalate (PEN), depositing all layers using RF magnetron sputtering. These devices present a staggered bottom gate, top contact structure and were fabricated as follows: Molybdenum (Mo) gate electrodes (≈ 60 nm thick) were deposited in an Ar atmosphere; for the dielectric a multilayer structure with alternating SiO_2 and co-sputtered $\text{Ta}_2\text{O}_5+\text{SiO}_2$ (denoted TSiO) layers was fabricated, with a thickness of 100-150 nm. The semiconductor, IGZO (≈ 40 nm thick and 2:1:1 In:Ga:Zn atomic ratio), was deposited in an Ar+ O_2 atmosphere. At the end, Mo source and drain electrodes were fabricated using the same procedure as for gate electrode. Both the electrodes and the semiconductor were patterned by lift-off and, on the other hand, the dielectric layer by dry-etching, in a SF_6 atmosphere. To conclude the production, the devices fabricated on glass and on PEN were annealed at 180-200 and 150 °C, respectively, on a hotplate, in air.

Electrical characterization of devices was performed using a semiconductor parameter analyzer (Keithley 4200-SCS) and a probe station (Cascade Microtech M150) under dark room conditions.

3.2 IGZO TFTs on Glass Substrate

As discussed in [15] a multilayer dielectric comprising TSiO and thin SiO_2 (with the latter being in contact with IGZO) results in considerably improved device yield over single layer TSiO or Ta_2O_5 . In fact, recent improvements in tuning the thickness of these multilayer dielectrics enabled breakdown field (E_{B}) > 7 MV/cm and $\kappa \approx 10$, resulting in IGZO TFTs with $I_{\text{G}} < 1$ pA and low operation voltage (yielding a transconductance saturation for $V_{\text{GS}} < 6$ V). Fig. 1 shows transfer and output curves of one IGZO TFT with a 150 nm thick multilayer dielectric comprising 7 alternating SiO_2 /TSiO layers, annealed at 180 °C, with a width-to-length ratio (W/L) of 40/20 (μm). Excellent performance is obtained: $\mu_{\text{FE}} \approx 14$ cm²/Vs, On-Off ratio $\approx 10^9$, $V_{\text{on}} = -1.5$

V , subthreshold slope (S) of 0.16 V/dec, negligible hysteresis, hard saturation and no current crowding at low V_{DS} . Note that these results are quite similar to the ones obtained when the same IGZO layers are deposited on state-of-the-art thermal dry SiO_2 . In fact, S and operating voltage are even improved with the present multilayer dielectric, owing to its larger κ (in thermal SiO_2 $S=0.20$ V/dec and transconductance saturation occurs for $V_{GS}=15$ V).

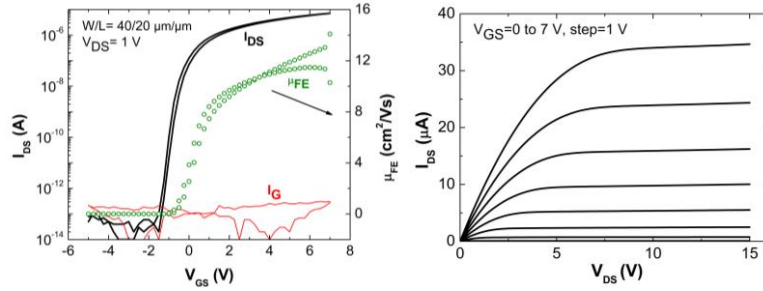


Fig. 1. Transfer (left) and output (right) curves of an IGZO TFT on glass with a sputtered 7 layer SiO_2/TSiO dielectric.

3.3 IGZO TFTs on Flexible PEN Substrate

The possibility of using flexible substrates brings significant advantages to a TFT technology. First, it enables the usage of roll-to-roll fabrication tools, highly desirable for large area electronics. Then, at a system level they enable weight and thickness reduction over conventional glass. Finally, bendable or even rollable products can be conceived. Given the low temperature fabrication required for IGZO TFTs with sputtered multilayer dielectrics, their performance was also analyzed on PEN substrates. Fig. 2 shows the transfer curves and a photo of such devices with a 7 layer dielectric, having a total thickness ≈ 100 nm, annealed at only 150°C . It is noteworthy the excellent electrical performance obtained: in fact, besides the larger hysteresis, all the other parameters reveal to be even slightly improved over the ones achieved on glass substrates (Fig. 1), which is also a consequence of the thinner dielectric layer used on PEN. Electrical characterization under different bending radius is currently underway.

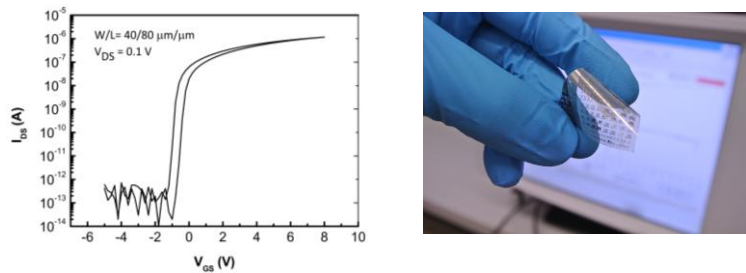


Fig. 2. Measured transfer curves (left) and a photo of IGZO TFTs on PEN substrate with $W/L=40/80$ $\mu\text{m}/\mu\text{m}$ and annealed at 150°C (right) using a multilayer dielectric (7 layers).

4 ADCs using Oxide TFTs Produced at FCT-NOVA

As mentioned before, circuit integration is a crucial demonstration of the potential of a new transistor technology. ADCs are one of the most difficult circuits to implement and, given their importance in a variety of fields such as electronic, medical, telecommunications or other systems that need signal processing, their implementation using a new technology is a significant achievement. Despite the lack of maturity compared to the dominant TFT technology (i.e., a-Si:H), oxide TFTs have been implemented in systems with a reasonable level of complexity and integration but, to the best of the authors' knowledge and up to date, no kind of reference was found regarding the use of oxide TFTs in the design and practical implementation of ADCs. Some works related with practical realizations of ADCs using other thin-film technologies are summarized in [16–18]. Although being a small part of all developed work, it contains examples of ADCs employing a-Si:H, low-temperature poly-silicon (LTPS) and organic TFTs.

Excellent performance, good stability, large E_B and low I_G are some of the key characteristics of IGZO TFTs with multilayer dielectric previously optimized, encouraging to proceed to the design of a 2nd-order Sigma-Delta ($\Sigma\Delta$) ADC using the devices produced at FCT-NOVA. An ADC architecture based on oversampling and noise-shaping techniques has been adopted, since due its intrinsic feedback nature, it can easily deal with high process variations and mismatch errors in the physical/electrical parameters of the TFT devices during fabrication. It is important to notice that, due to the lack of a reproducible and stable p-type oxide TFTs, only n-type devices were used in the circuit design. Additionally, due to the expected high device mismatch and poor absolute accuracy when these passive elements are fabricated, SMD passive elements have been employed in order to minimize additional risks in the early phase of proof-of-concept.

VirtuosoTM Platform and SpectreTM Simulator from CADENCE have been used to design and electrically simulate all building blocks. Furthermore, a model for IGZO TFTs was adapted from an a-Si:H TFT model developed by Semiconductor Devices Research Group at RPI, with good fitting to experimental data.

Given the relevance of the comparator in the $\Sigma\Delta$ modulator ($\Sigma\Delta M$), the active block in circuit, it was designed and simulated in order to obtain the best performance. It employs a cascade of three pre-amplification stages, a positive-feedback analog latch stage and four logic inverters implementing a fully-dynamic digital latch. Results show a low offset, working at several tens of kHz, with an accuracy ≈ 10 mV. Moreover, it supports the V_{on} variations of fabrication [19].

Regarding the final design of continuous-time $\Sigma\Delta M$, it employs an analog loop filter (a cascade connection of two fully passive RC-type integrators), implementing the 2nd-order noise shaping transfer function. ADC simulations reveal: SNDR ≈ 57 dB, DR ≈ 65 dB, and power dissipation, approximately, of 22 mW ($V_{DD} = 10$ V). Comparing these simulation results, shown in Table 1, with the current state-of-the-art of $\Sigma\Delta M$ s, it can be observed that this work is clearly beyond prior art, for competing thin-film technologies such as organics or even LTPS, supporting the continuity of this work. However, the operation frequency and intrinsic gain of these devices can limit the performance of the $\Sigma\Delta M$. Nevertheless, results give an excellent stimulus to produce one of the first 2nd-order $\Sigma\Delta$ ADC using oxide TFTs.

Another paramount step in this kind of work is the layout, specially using new technologies for which a process-design-kit (PDK) is not available. Consequently, a parameterized cell (PCELL) needs to be constructed taking into account the structure of devices and all process/material constraints. Given the absence of PDK, automatic design rule check (DRC) and layout versus schematic (LVS) could not be performed using EDA (electronic design automation) tools. Hence, layout of the entire circuit with a die area close to 10 mm² still needs to be checked manually. More details regarding design, simulation results and layout can be found in [15].

Table 1. Simulated main performance parameters of the $\Sigma\Delta$ using IGZO TFTs.

Characteristic	Value
Sampling Frequency (F_s)	128 kHz
Input Signal Amplitude (A_{in})	5 V _{diff}
Input Signal Frequency (F_{in})	101.5625 Hz
Oversampling ratio (OSR)	128
Bandwidth (BW)	500 Hz
Signal-to-noise distortion ratio (SNDR)	57 dB
Dynamic Range (DR)	65 dB

5 Conclusions

Fully sputtered IGZO TFTs have been produced both on glass and PEN exhibiting comparable electrical performance, with $\mu_{FE} \approx 14$ cm²/Vs, On-Off ratio $\approx 10^8$ - 10^9 , $V_{on} = -1.0$ to -1.5 V and subthreshold slope (S) of 0.16 V/dec. These properties are achieved with only 150-180 °C annealing temperature and are even superior to the ones obtained with high-temperature 100 nm thick dry-SiO₂ dielectric from conventional CMOS technology. A 2nd-order $\Sigma\Delta$ was designed and simulated based on the measured IGZO TFTs, showing a SNDR ≈ 57 dB, and a power dissipation of 22 mW. Circuit layout with a die area of 10 mm² is currently under final LVS and DRC verifications. Fabrication and experimental evaluation will be the next steps.

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