A Switched-Capacitor Band-Pass Biquad Filter Using a Simple Quasi-unity Gain Amplifier

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Abstract. This paper presents a switched-capacitor (SC) band-pass biquad using a simple quasi-unity gain amplifier. In sub-nanometer CMOS technologies the intrinsic gain of the transistors is low; this increases the difficulty of designing high gain amplifiers. The proposed SC filter is based on the Sallen-Key biquad and it requires only a simple low gain amplifier. A differential filter circuit, including a suitable amplifier based on a fully-differential voltage-combiner is presented and analyzed. The correct functionality of this circuit is validated through electrical simulations of a second-order band-pass filter. These simulations show that, for a clock frequency of 100 MHz, the frequency response of the circuit is similar to the corresponding prototype filter.

Keywords: Analog circuits, band-pass Sallen-Key, switched-capacitor circuits, voltage-combiner amplifier.

1 Introduction

Analog filters are extremely important blocks in several electronic systems, such as RF transceivers or sigma delta modulators. They allow selecting between signals with different frequency and eliminating unwanted signals.

The scaling-down of transistors in advanced deep-submicron CMOS technologies results in the reduction of the intrinsic gain (g_m/g_{ds}) [1] and in an increase in the variability, making the design of high gain amplifiers increasingly difficult, especially for larger bandwidths. This limitation has large impact in the performance of filter circuits.

This paper proposes the design of filter circuits using low gain amplifiers, in order to avoid the difficulty of designing high gain amplifiers with large bandwidth. The SC filter circuit described in this paper is based on a band-pass Sallen-Key biquad [2] which does not require high gain amplifiers. This filter topology simplifies the design of the amplifier although it also eliminates the virtual ground node from the circuit. Without this node, parasitic insensitive SC branches cannot be used. Due to modern parasitic extraction software which can reliably predict the values of parasitic capacitances, the historical disadvantage of parasitic sensitive SC branches (parallel SC) is no longer critical, thus allowing their influence to be compensated during the design phase of the filter.

The paper is organized as follows. As required, Section 2 shows the relationship between the work presented in this paper and the Internet of Things topic. Section 3 shows a brief state of the art about typical SC circuits. Section4 describes and analyzes the biquadratic (biquad) section implemented in this paper. Section5 describes and analyzes the low gain amplifier used in the biquadratic section. In Section6 the simulation results of second-order band-pass SC filter are given. Section7 draws the main conclusions from the work carried out in this paper.

2 Relationship to Internet of Things

To have an Internet of things it is necessary to have electronic systems associated to objects (things) that need to be connected to the Internet. In order for these systems to be smaller and to have a lower cost, it is important to use the concept of system-on-a-chip (SoC). This means that a single die is used to build the entire system thus reducing the size, cost, and power dissipation of the system.

The technology used in a SoC is selected in order to maximize the performance of the digital circuits of the system; this means that the analog circuits in the system have to be designed using advanced nanometer (nm) CMOS technologies. This can be a problem because the transistors in these technologies are not optimized for working in analog circuits; in particular they have low intrinsic gain which makes the design of high gain amplifiers particularly difficult. This paper, describes the design of a band-pass filter using low gain amplifiers, which facilitates the use of advanced nm CMOS technologies, thus addressing one of the problems associated to the Internet of things.

3 Switched Capacitor Circuits

Interests in SC networks started in the late 70s due to the possibility of implementing analog filters using monolithic integrated circuit (IC) technology and because it is possible to obtain a good accuracy in the ratio between two capacitor values, as opposed to the low accuracy of the absolute values of resistors and capacitors. Also, since a high value resistor can be generated using small on-chip capacitors and a high frequency clock, the area occupied by a SC filter in an integrated circuit is typically smaller than the area occupied by an equivalent RC filter.

SC circuits can be implemented using different types of SC branches some of which, when using high gain amplifiers, are insensitive to parasitic capacitances [3][4]. However, this type of approach becomes harder to implement with the decrease of the intrinsic gain of transistors.

4 Biquadratic Sallen-key Based Circuit

The single-ended configuration of the band-pass SC Sallen-Key based topology is shown in Fig.1. This circuit is obtained by replacing the resistors with parallel SC branches in the band-pass Sallen-Key circuit. An additional capacitor (C_3) was added to the circuit to facilitate the process of compensating the input parasitic capacitance of the amplifier.

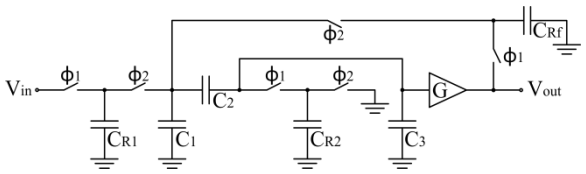

Fig.1. Band-pass SC biquad filter in single-ended configuration.

The transfer function (1) was obtained from the analysis of the previous circuit from a charge conservation perspective, considering that the circuit's output is sampled at the end of phaseΦ_1.

$$H(z) = V_{out}(z)/V_{in}(z) = G\,(z-1)d/(a - b\,z + c\,z^2) \tag{1}$$

where,

$$a = \big(C_1(C_2 + C_3) + C_3(C_{R1} + C_{Rf}) + C_2(C_3 + C_{R1} + C_{Rf})\big)\big(C_2(C_3 + C_{R2}) + C_1(C_2 + C_3 + C_{R2})\big)$$

$$b = C_1\big(C_3^2(C_{R1} + C_{Rf}) + C_2^2(4C_3 + C_{R1} + C_{R2} + C_{Rf} + G\,C_{Rf}) + C_2C_3(2(2C_3 + CR1{+}CR2{+}CRf{+}G\,CRf{+}C12C2{+}C32C2{+}C3{+}CR2 \tag{2}$$

$$c = \big(C_2(C_3 + C_{R2}) + C_1(C_2 + C_3 + C_{R2})\big)\big(C_1(C_2 + C_3) + C_3(C_{R1} + C_{Rf}) + C_2(C_3 + C_{R1} + C_{Rf})\big)$$

$$d = G\big(C_2C_3 + C_1(C_2 + C_3)\big)C_2C_{R1}$$

Since the filter is implemented using parasitic sensitive branches, the capacitor values must be adjusted to compensate for the parasitic capacitances present in the circuit. Fig.2shows the filter schematic considering these parasitic capacitances introduced by the switches and the amplifier.

Because all parasitic capacitances are in parallel with existing capacitors, their influence can be directly compensated by changing the values of these capacitors. The compensated capacitor values of filter in consideration can be obtained from (3).

$$C_{1x} = C_1 - C_{M2s} - C_{M5d} \qquad C_{3x} = C_3 - C_{Bin} - C_{M3d} \qquad C_{Rfx} = C_{Rf} - C_{M5s} - C_{M6d} \tag{3}$$

$$C_{R1x} = C_{R1} - C_{M1s} - C_{M2d} \qquad C_{R2x} = C_{R2} - C_{M3s} - C_{M4d}$$

An approximation of the parasitic capacitances of the switches and of the input capacitance of the amplifier is obtained from the DC simulation of the circuit. The drain capacitance of transistor M_1 is neglected since it doesn't alter the circuits transfer function. The amplifier's output capacitance can also be neglected since it is connected to a low impedance node.

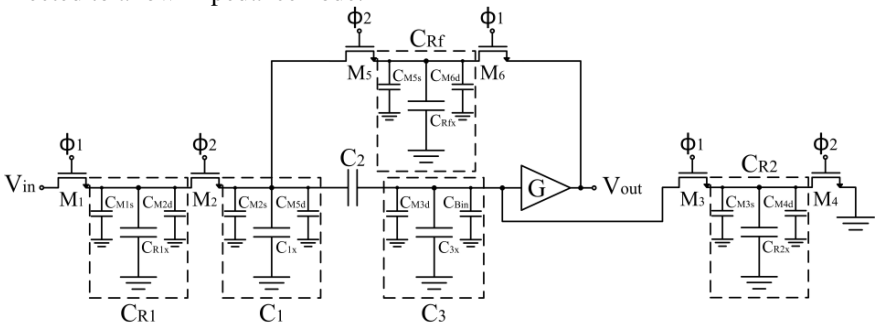

Fig.2. Band-pass SC filter in single-ended configuration considering parasitic capacitances.

In order to cancel the even harmonics and reduce the distortion due to charge injection from the switches, the differential configuration was obtained (Fig.3). Assuming that in this configuration the voltage drop across the capacitors is two times larger than in the single-ended configuration, the capacitors must have half the capacitance of the single-ended capacitors.

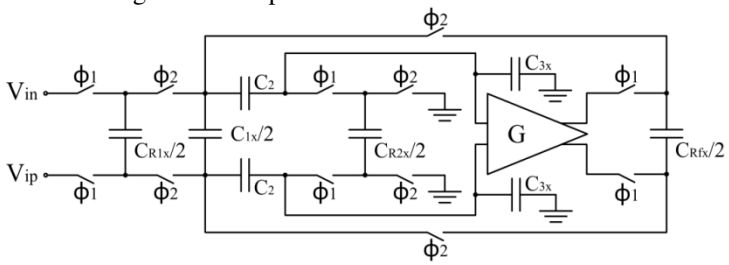

Fig.3. Band-pass SC filter in differential configuration.

Note that in order to maintain the common mode voltage relatively constant within the circuit, $C_{R2x}/2$is connected to this common mode voltage during phase Φ_2 instead of ground.

5 Voltage-Combiner Amplifier

The single-ended configuration of the voltage-combiner amplifier is shown Fig. 4. Notice that M_1 and M_2 devices act, respectively, as common-source and common-drain devices.

In single-ended configuration this circuit acts as buffer and has a gain below unity. Doubling the circuit and connecting the sources of transistor M_1 (node V_{dif}), a differential pair is formed and the circuit becomes a low gain amplifier.

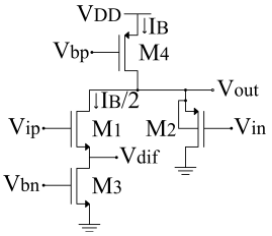

Fig. 4. Voltage-combiner in single-ended configuration.

The low frequency open-loop gain of the circuit shown in Fig. 4 is given by:

$$G = \frac{g_{m1}g_{ds3} + g_{m2}(g_{m1} + g_{mb1} + g_{ds1} + g_{ds3})}{(g_{m2} + g_{ds2} + g_{ds4})(g_{m1} + g_{mb1} + g_{ds3}) + g_{ds1}(g_{m2} + g_{ds2} + g_{ds3} + g_{ds4})} \quad (4)$$

In order to improve the linearity of the amplifier, a small amount of source degeneration is used[5]-[7] in the differential pair formed by common-source transistors M_1, as shown in Fig. 5, using two MOS transistors operating in the triode region ($M_5$and M_6) which exhibit higher linearity than transistors operating in the saturation region. The gain of this circuit can be easily adjusted, through design, to vary between 0.879 and 1.637, for a common mode voltage of 600 mV.

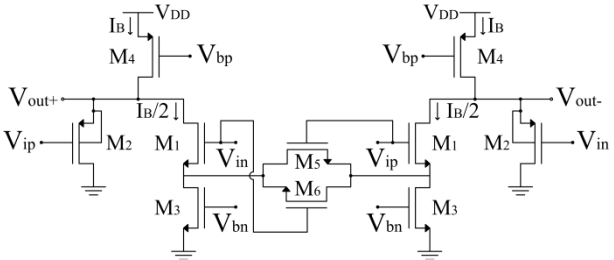

Fig. 5. Voltage-combiner with source degeneration using MOS transistors.

Depending on the width used on transistors M_5 and M_6, the gain of the amplifier and its linearity will vary. To improve the amplifiers linearity, the width of both transistors should be lowered (increasing r_{ds}) until the optimum point is found. As a consequence the gain of the amplifier will decrease with the decrease of these transistors width. Since lowering the gain makes the design of the filter harder, the widths of M_5 and M_6 were chosen so that the gain is larger than 1.2. The simulated gains of the amplifiers are shown in Fig. 6 and Fig. 7.

The amplifier was sized in order to maximize both gain and GBW. The sizing used is shown in Table 1.

Table 1. Transistor sizes used in the voltage-combiner amplifier.

Devices	M_1	M_2	M_3	M_4	M_5 and M_6
W [µm]	16	21.36	4.8	24	20
L [nm]	120	120	120	120	120

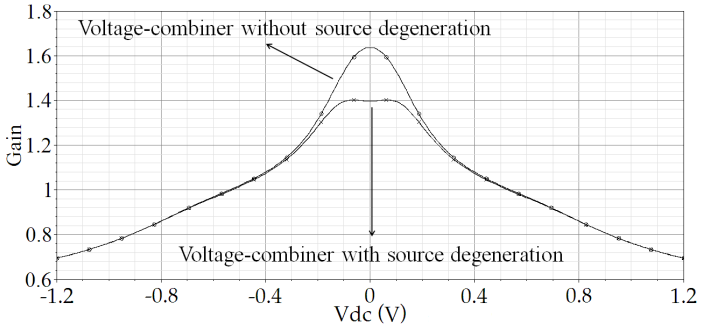

Fig. 6. Low-frequency gain of the voltage-combiner amplifier as a function of the differential input voltage.

The frequency response of the amplifier is shown in Fig. 7.

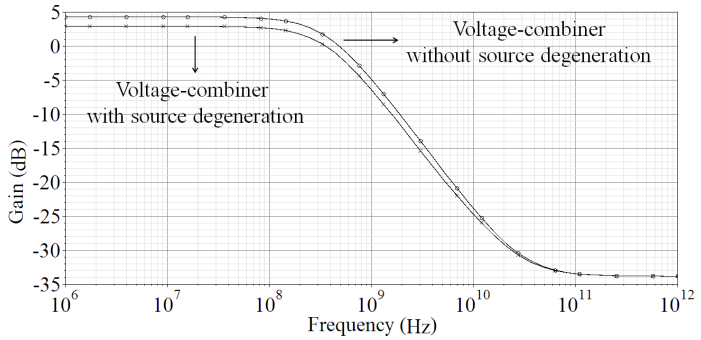

Fig. 7. Bode diagram (amplitude) of the voltage-combiner amplifier.

6 Simulation Results

The biquadratic section described in Section4 and the amplifier from Section 5 were designed in a standard 1.2 V 130 nm CMOS technology, in order to implement a biquadratic second-order band-pass Butterworth SC filter, with a central frequency of 1 MHz, a pass band of 500 kHz, and a clock frequency of 100 MHz.

The current drawn by the amplifier is determined in order for the settling error to be below 0.1%. To achieve this, it is necessary to have a certain gain-bandwidth product (GBW) that can be calculated from (5). Since the clock frequency is 100 MHz, the GBW of the amplifier has to be higher than 220 MHz to ensure a settling

error below 0.1%. The transistors sizes used for the voltage-combiner amplifier that are shown in Table 1 were chosen in order to satisfy the following condition.

$$e^{-GBW[rad/s]T_s/2} < 0.1\% \Leftrightarrow GBW[Hz] > -\ln(0.1\%)F_s/\pi \quad (5)$$

Based on the gain of the voltage-combiner amplifier, the filter was initially designed from an ideal standpoint (assuming ideal switches, capacitors and amplifier) and then using the parasitic capacitances values obtained from an operating bias point (DC) simulation of the real circuit, the parasitic capacitances were compensated. Table 2 shows the values of the capacitors used in the single-ended configuration of the filter and the values of the parasitic capacitances. Note that the values of the parasitic capacitances are an approximation since due to the common mode voltage variation within the filter, these capacitance values will slightly vary.

Table 2. Filter gain, parasitic capacitances and single-ended capacitor values.

Gain [V/V]	**C_1 [pF]**	**C_2 [pF]**	**C_3 [fF]**	**C_{R1} [fF]**	**C_{R2} [fF]**	**C_{Rf} [fF]**	**C_{Bin} [fF]**	**C_{pd} [aF]**	**C_{ps} [aF]**
1.3965	2	4	300	72.56	90.26	491.75	68	160.34	150.59

To determine the frequency response of the SC filter, an impulse is applied to the input, allowing charge into the circuit exclusively during one single clock phase (Φ_1), charging capacitors. Using this input causes the circuit to produce its impulse response. This signal is then sampled at intervals of $1/F_s$, at the end of clock phaseΦ_1, until the impulse response is zero. These samples can be used to compute the frequency response of the filter shown in Fig.3.

The frequency responses of the prototype filter, ideal circuit, and real circuit of the second-order filter are shown in Fig. 8. The attenuations at the filter bandwidth, as well as the amplifier's parameters and IM2 distortions are shown in Table 3.

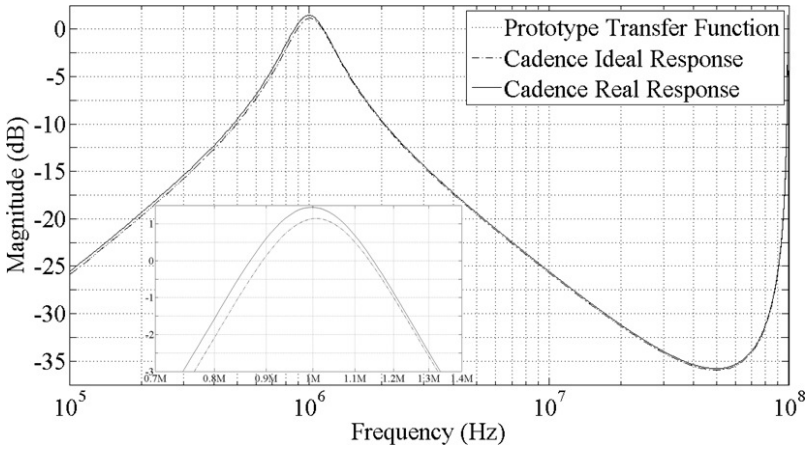

Fig. 8. Frequency response of the second-order band-pass filter.

Table 3. Simulation results.

Filter Attenuation @ Filter Bandwidth			**Voltage-Combiner Amplifier**		**IM2 @ 200 mV_{pp}**	
Prototype [dB]	-2.58	-2.29	**DC Gain [dB]**	2.90	**Real**	
Ideal Circuit [dB]	-2.58	-2.29	**Power [µW]**	244.33	**Circuit**	-52.11
Real Circuit [dB]	-2.07	-2.17	**GBW [MHz]**	349.8	**[dB]**	

7 Conclusion

This paper presented a solution to implement SC band-pass filters without the need of high gain amplifiers. The solution proposed using a low gain voltage-combiner amplifier and parasitic sensitive branches that, due to not having a virtual ground node in the circuit, require the compensation of parasitic capacitances during the design process. This technique simplified the design of the amplifier, reducing the total power consumption, and the silicon area of the overall filter. Simulation results, of the second-order band-pass SC filter, showed that for a clock frequency of 100 MHz, it's possible to obtain a frequency response similar to the one using ideal components. During the simulation phase it was seen that most of the distortion of the filter is introduced by the amplifier circuit, making it necessary to use other techniques, in addition to source degeneration, in order to reduce the distortion introduced by this circuit and also to make it less sensitive to process variation.

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