Analysis and Design Strategy of On-Chip Charge Pumps for Micro-Power Energy Harvesting Applications

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Abstract. Charge balance law based on conservation of charge is stated and employed to analyze on-chip linear, Fibonacci and exponential charge pumps. For micro-power on-chip implementations, both the positive- and the negative-plate parasitic capacitors have to be considered. Voltage conversion ratios and efficiencies can be obtained in closed form for single- and dual-branch linear charge pumps, but not for Fibonacci and exponential charge pumps. Instead, a first iteration approximation analysis for computing voltage conversion ratio is proposed. For the linear charge pump, efficiency optimization is achieved by first computing the optimal number of stages, and then obtaining from the required output voltage the reduction factor that is a function of load current, flying capacitor and switching frequency. Using a 0.35μm CMOS process, 8X linear, Fibonacci and exponential charge pumps are designed and their performances are compared and confirmed by extensive Cadence Spectre simulations. It is concluded that linear charge pumps attain the best efficiency.

Keywords: charge balance, charge pump, charge redistribution, exponential charge pump, Fibonacci charge pump, linear charge pump

1 Introduction

Micro-power energy harvesting and micro-sensor applications require fully on-chip implementation of power management units that include integrated switched-capacitor power converters, or charge pumps (QPs). Embedded systems that have a stringent silicon estate need fully on-chip charge pumps for reading and writing EEPROM. For on-chip charge pumps, efficiency in power and area are two major concerns, and both are closely related to charge pump topologies that determine the number of capacitors and switches and losses due to parasitic capacitors. Integrated linear (or Dickson) charge pumps (LQPs) are the most popular implementations due to their simple structure and readily available design procedures [1-8]. With a 2-phase non-overlapping clock, the Fibonacci charge pump (FQP) [9] and the exponential charge pump (EQP) [10, 11] promised to achieve very high voltage conversion ratios using fewer capacitors than the LQP, and both are potential candidates for on-chip applications. Therefore, there is a practical need in analyzing which charge pump would have the best efficiency using the smallest area of on-chip capacitors.

Consider a (linear) charge pump with N flying capacitors and a load capacitor. For each flying capacitor C_k (the k^{th} stage), one plate is always at a higher potential and is called the positive plate, while the other is the negative plate. For an on-chip capacitor C_k, both the positive-plate and negative-plate parasitic capacitors can be considered to be proportional to C_k, namely, αC_k and βC_k, respectively, and they are not negligibly small. In [2], the output voltage V_o was derived by assuming that all C_k are equal and the load capacitor C_L is infinite, and equal C_k gives the smallest total capacitance in maximizing V_o [1]. The exact argument of how to charge up an infinite capacitor was not presented, and the efficiency was not considered. The Dickson derivation of [2] used heuristic reasoning in accounting for αC_k and formed the basis of many subsequent analyses [3-8]. Evidently, a more solid derivation on par with circuit analysis using Kirchhoff's current and voltage laws is needed. In [3], the authors commented that the output voltage ripple ΔV_o could be added back to the case with $C_L=\infty$, but gave no computation details. Nevertheless, the major concern of [3] (and [8]) was to compute the non-ideal effect of the transistor switches. In [4], both the load capacitor and the parasitic capacitors were not considered in analyzing the Dickson charge pump, and no efficiency information was given. In [5] (and [7], an extended version of [5]), the correct equation for the output voltage of an ideal linear charge pump with different C_k and an infinite C_L was put down without elaboration. More importantly, it presents a design procedure that minimizes the input current, which is equivalent to maximize the power conversion efficiency η. However, αC_k are ignored in [5] as the authors argue that the major contributions of loss are from βC_k. To improve the analysis of [5], both αC_k and βC_k are included in [6], but it assumes that all αC_k are charged in both phases, while in the steady state, any capacitor should have alternate charging and discharging phases in one cycle. Despite the deficiencies, [5] and [6] are among the very few publications that presented formulae for computing efficiency. While analyses of LQPs are numerous, there is no corresponding analysis for FQPs and EQPs, and they could not be easily analyzed by the Dickson derivation.

In this research, the linear charge pump with parasitic capacitors and a finite load capacitor is analyzed. Ideal switches are assumed, as non-ideal switches lead to incomplete charge transfer that should be dealt with in a separate work. Analysis on charge transfer and charge redistribution is based on systematic application of the charge balance law (QBL) to be discussed in Section 2 [12, 13]. The output voltage $V_o(t)$ and the average output voltage V_o are derived in Section 3, the power conversion efficiency η in Section 4, and V_o and η of the dual-branch linear charge pump in Section 5. Cadence Spectre simulation results of single- and dual-branch linear charge pumps are presented in Section 6. The first iteration approximation analysis is employed in analyzing Fibonacci and exponential charge pumps in Section 7 and Section 8, respectively [14]. All charge pumps are compared in Section 9. After concluding that the linear charge pump is the most efficient on-chip implementation with the smallest area, a detail design strategy is proposed in Section 10, followed by some concluding remarks in Section 11.

2 Charge Balance Law

In circuit analysis, we use Kirchhoff's current law and Kirchhoff's voltage law systematically to solve problems. It is beneficial to have a similar law for analyzing switched-capacitor circuits including charge pumps. In fact, to facilitate the computation of charge transfer, a law that is based on conservation of charge can be formulated. The **charge balance law** (**QBL**) says

> ***In a system of capacitors, the sum of all charges leaving a node at any instance of charge transfer is equal to zero.***

It is obvious that the term "leaving a node" can be replaced by "entering a node" with the same validity. This law was first named Kirchhoff's charge law in [12] and then in [13], but is better be renamed as the charge balance law. It is also known simply as charge balance in [15]. Fig. 1 shows n capacitors (C_1, C_2, …, C_n) to be connected at the node V_a at $t=t_o$. For each capacitor, one plate will be connected to V_a and let us arbitrarily assign that plate to be the positive plate, while the negative plate will be connected to other circuit components not shown. Prior to the charge transfer, the corresponding capacitor voltages are $V_{C1}(t_o^-)$, $V_{C2}(t_o^-)$, …, $V_{Cn}(t_o^-)$, and at $t=t_o$, charge transfer occurs, such that when charge redistribution is completed, the capacitor voltages are $V_{C1}(t_o^+)$, $V_{C2}(t_o^+)$, …, $V_{Cn}(t_o^+)$. Employing QBL we have

$$\sum_{k=1}^{n} C_k V_{Ck}(t_o^-) = \sum_{k=1}^{n} C_k V_{Ck}(t_o^+) \; . \tag{1}$$

A simple way to apply QBL is to remember

$$\text{Total Initial Charge} = \text{Total Final Charge.} \tag{2}$$

In this paper, all equations accounting for charge transfer are written in the form of (2).

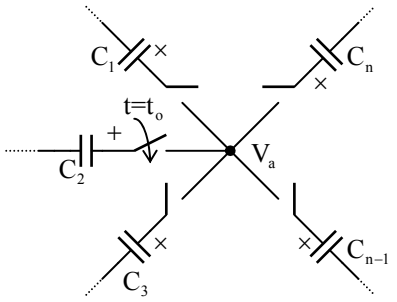


Fig. 1. Charge redistribution at the node V_a.

3 Analysis of Single-Branch Linear Charge Pumps

Fig. 2 shows a single-branch N-stage linear charge pump (LQP) with a voltage conversion ratio M (=V_o/V_{dd}) that is equal to N+1 if the load current is zero. The analysis is simplified by having a load current I_o instead of a load resistor. The case using ideal switches and no parasitic capacitor has been derived in [13]. We now turn to the general case that any on-chip (flying) capacitor C_k has both positive-plate and negative-plate parasitic capacitors αC_k and βC_k to ground.

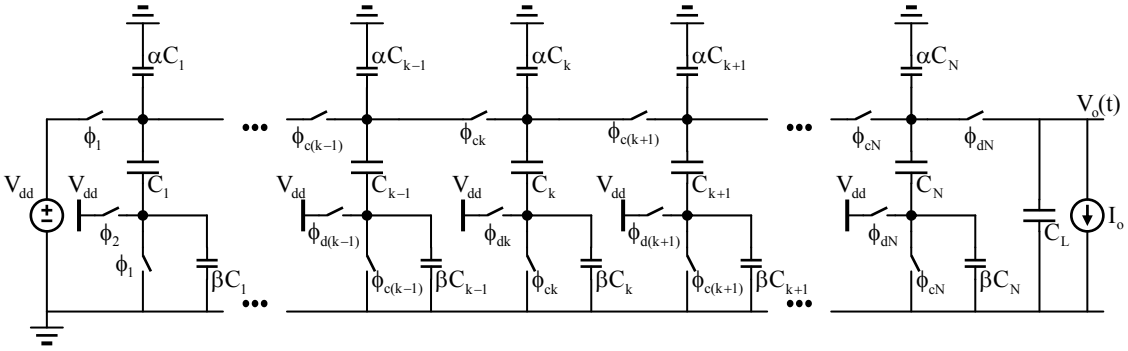


Fig. 2. Single-branch (N+1)X linear charge pump with parasitic capacitors.

Fig. 3 shows the voltages across the capacitors C_k, αC_k and C_L. Every capacitor C_x has a charging phase ϕ_{cx} and a discharging phase ϕ_{dx}. For example, for k even, the charging phase of C_k is $\phi_{ck}=\phi_2$. We assign V_k as the capacitor voltage of C_k (at the end) of its discharging phase. The analysis of charge pumps involves mundane charge accounting, and our experience tells us that it is more efficient to work from the output side towards the input side. Fig. 3(d) shows the time-varying output voltage $V_o(t)$, and let V_{o1} be the output voltage at the beginning of the discharging phase of C_N ($\phi_{dN}=1$). During $\phi_{dN}=1$, the load current I_o discharges C_N and C_L for half of the clock period T/2, and

$$V_{o1} = V_{o2} + \frac{I_o T/2}{(1+\alpha)C_N + C_L}. \tag{3}$$

During the next phase $\phi_{cN}=1$, C_N is disconnected from C_L, and the load current discharges C_L and gives

$$V_{o3} = V_{o2} - \frac{I_o T/2}{C_L}. \tag{4}$$

The output voltage ripple ΔV_o is immediately given by

$$\Delta V_o = V_{o1} - V_{o3} = \frac{I_o T}{2} \frac{1}{C_L \,||\, [(1+\alpha)C_N + C_L]}. \tag{5}$$

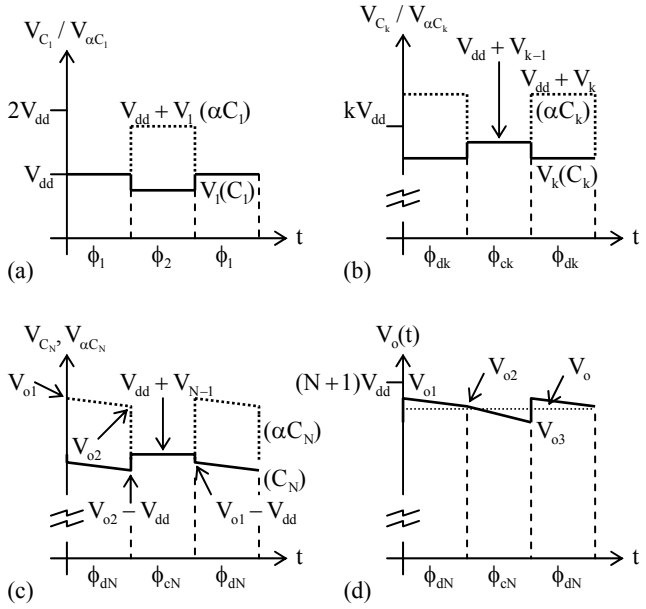


Fig. 3. Capacitor and output voltages of LQP: (a) V_{C1} and $V_{\alpha C1}$; (b) V_{Ck} and $V_{\alpha Ck}$; (c) V_{CN} and $V_{\alpha CN}$; and (d) $V_o(t)$.

While C_L is discharged by I_o, C_N is being charged up, and the charging phase of C_N is the discharging phase of C_{N-1}. Therefore, in $\phi_{cN}=1$, C_{N-1} is discharged to V_{N-1}, C_N is charged to $V_{dd}+V_{N-1}$, and αC_N is discharged to $V_{dd}+V_{N-1}$. In fact, it will become clear later that while the flying capacitor C_k is being charged up, αC_k is being discharged (Fig. 4). At the start of the next clock phase, that is, at the instant of $\phi_{dN}=1$ again, C_N redistributes charge with C_L such that $V_o(t)$ is pumped up from V_{o3} to V_{o1}. Employ QBL gives

$$(1+\alpha)C_N(V_{dd}+V_{N-1})+C_L V_{o3}=C_N(V_{o1}-V_{dd})+\alpha C_N V_{o1}+C_L V_{o1}. \tag{6}$$

In substituting (3) and (4) into (6) we have

$$V_{o2}=\frac{2+\alpha}{1+\alpha}V_{dd}+V_{N-1}-\frac{I_o T}{(1+\alpha)C_N}. \tag{7}$$

Next, consider the charge redistribution of C_{N-1} with C_N, and QBL gives

$$\begin{aligned}(1+\alpha)C_{N-1}(V_{dd}+V_{N-2})+C_N(V_{o2}-V_{dd})+\alpha C_N V_{o2}=\\ C_{N-1}V_{N-1}+\alpha C_{N-1}(V_{dd}+V_{N-1})(1+\alpha)C_N(V_{dd}+V_{N-1})\end{aligned}. \tag{8}$$

In making use of (7), (8) can be simplified to

$$V_{N-1}=\frac{1}{1+\alpha}V_{dd}+V_{N-2}-\frac{I_o T}{(1+\alpha)C_{N-1}}. \tag{9}$$

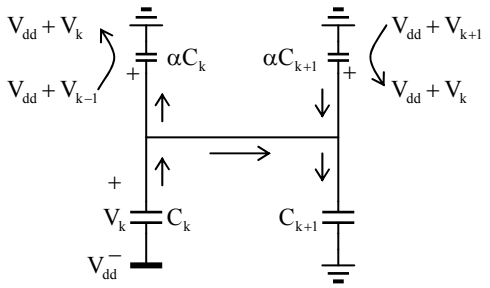


Fig. 4. Capacitor C_k in discharging phase.

We then consider the general k^{th} stage, such that C_k is charged up by C_{k-1} in its charging phase ϕ_{ck}, and redistributes charge with C_{k+1} during its discharging phase ϕ_{dk}. Employ QBL and an equation similar to (8) can be written down. By grouping the terms involving C_k and C_{k+1} on different side we obtain

$$C_k V_{dd} + (1+\alpha)C_k V_{k-1} - (1+\alpha)C_k V_k = C_{k+1}V_{dd} + (1+\alpha)C_{k+1}V_k - (1+\alpha)C_{k+1}V_{k+1}\,. \tag{10}$$

An immediate relation is revealed if we consider k=N–2 such that the right hand side of (10) is equal to I_oT, and (10) is the same as (9) with a different index. Clearly, the same relation propagates down the charge pump, and we can rewrite (10) as

$$V_k = \frac{1}{1+\alpha}V_{dd} + V_{k-1} - \frac{I_oT}{(1+\alpha)C_k}\,. \tag{11}$$

However, C_1 has no prior stage, and V_0 (not V_o) is zero, that is,

$$V_1 = \frac{1}{1+\alpha}V_{dd} - \frac{I_oT}{(1+\alpha)C_1}\,. \tag{12}$$

The interpretation of (11) is that the overall change in charge of each flying capacitor in one cycle is the amount of charge I_oT delivered to the adjacent higher stage in the same cycle. This charge transfer is independent of C_L. Consider that when C_k is charged to $V_{dd}+V_{k-1}$, the voltage across αC_k is also $V_{dd}+V_{k-1}$. When C_k is discharged to V_k, the voltage across αC_k is $V_{dd}+V_k$. It is clear from (11) that $V_{dd}+V_k$ is larger than $V_{dd}+V_{k-1}$. Hence, when C_k is being charged, αC_k is being discharged, but in [6], αC_k is assumed to be charged in both phases. Next, substitute (9), (11) and (12) into (7), and we have

$$V_{o2} = \frac{N+1+\alpha}{1+\alpha}V_{dd} - \sum_{k=1}^{N}\frac{I_oT}{(1+\alpha)C_k}\,. \tag{13}$$

An important observation is that V_{o2} is independent of C_L, and this property is very useful in simplifying the analysis for the case of $C_L=\infty$. From V_{o2}, one can write down V_{o1} and V_{o3} from (3) and (4) easily:

$$V_{o1} = \frac{N+1+\alpha}{1+\alpha}V_{dd} - \sum_{k=1}^{N}\frac{I_oT}{(1+\alpha)C_k} + \frac{I_oT/2}{(1+\alpha)C_N + C_L}\,, \tag{14}$$

$$V_{o3} = \frac{N+1+\alpha}{1+\alpha} V_{dd} - \sum_{k=1}^{N} \frac{I_o T}{(1+\alpha)C_k} - \frac{I_o T/2}{C_L} . \tag{15}$$

The average output voltage can be computed from Fig. 3(d) by averaging the areas of trapezoids as $V_o = (V_{o1}+2V_{o2}+V_{o3})/4$, that is,

$$V_o = \frac{N+1+\alpha}{1+\alpha} V_{dd} - \sum_{k=1}^{N} \frac{I_o T}{(1+\alpha)C_k} - \frac{I_o T}{8}\left(\frac{1}{C_L} - \frac{1}{(1+\alpha)C_N + C_L} \right). \tag{16}$$

A practical capacitance assignment requires $C_L > C_k$, and usually, $C_L >> C_k$, and the effect of C_L is negligibly small; or equivalently, we may assume $C_L \to \infty$, such that $V_o = V_{o2}$. To maximize V_{o2} ($\approx V_o$) and minimize the total capacitance C_T it is clear that all C_k should be set equal [1, 13]:

$$C_1 = C_2 = ... = C_N = C . \tag{17}$$

The total capacitance C_T is

$$C_T = NC , \tag{18}$$

and the output voltage and the output voltage ripple (with $C_L >> C_k$) are then given by

$$V_o = \frac{N+1+\alpha}{1+\alpha} V_{dd} - \frac{N I_o T}{(1+\alpha)C} , \tag{19}$$

$$\Delta V_o = \frac{I_o T}{C_L} . \tag{20}$$

Let us define the reduction factor δ as the fractional voltage drop per stage due to the load current I_o with the flying capacitor equal to C:

$$\delta = \frac{I_o T}{C V_{dd}} . \tag{21}$$

The voltage conversion ratio M can then be written as

$$M = \frac{V_o}{V_{dd}} = \frac{N+1+\alpha-N\delta}{1+\alpha} . \tag{22}$$

As α (as well as β) is fixed in a fabrication process, the only way to increase the output voltage V_o ($=MV_{dd}$) is to use a small δ, that is, to use a large C or a high switching frequency f_s ($=1/T$) as design constraints allow. In Section 4, we will show that this criterion is in conflict with maximizing the efficiency in the presence of parasitic capacitors.

4 Efficiency Optimization of Linear Charge Pumps

After obtaining the output voltage as a function of capacitors, switching frequency and load current, the next is to compute and optimize the efficiency η. Let E_i be the input energy supplied by V_{dd} in one cycle, and E_o the output energy consumed by the load in the same cycle. The efficiency of a charge pump is given by

$$\eta = \frac{E_o}{E_i}. \tag{23}$$

The term E_o is simply given by

$$E_o = V_o I_o T. \tag{24}$$

With reference to Fig. 2, the term E_i supplied by V_{dd} can be divided into three types: (1) E_{i1} is the cycle energy delivered to the positive plates of C_1 and αC_1 when being charged; (2) E_{i2k} is the cycle energy delivered to the negative plate of C_k when it is discharged; and (3) E_{i3k} is the cycle energy delivered to the positive plates of βC_k when being charged. Hence,

$$E_i = E_{i1} + \sum_{k=1}^{N} E_{i2k} + \sum_{k=1}^{N} E_{i3k}. \tag{25}$$

First of all, consider C_1 being charged by V_{dd}. With reference to Fig. 3(a), when C_1 is previously discharged to V_1, αC_1 is charged to $(V_{dd}+V_1)$. In the charging phase of C_1, if we assume there is no reversion loss, that is, the charge $\alpha C_1(V_{dd}+V_1)$ entirely redistributes with C_1 first before C_1 is charged by V_{dd}, then the charge ΔQ_{i1} supplied by V_{dd} is

$$C_1 V_1 + \alpha C_1 (V_{dd} + V_1) + \Delta Q_{i1} = (1+\alpha) C_1 V_{dd}. \tag{26}$$

Using (12) and that E_{i1} is equal to $V_{dd}\Delta Q_{i1}$, we have

$$E_{i1} = V_{dd} I_o T. \tag{27}$$

In computing E_{i2k}, denote the charge that is lost on the positive plate of C_k in its discharging phase as ΔQ_{i2k}, and this charge has to be supplied by V_{dd} to the negative plate of C_k. Hence, for C_k ($k \neq N$), we have

$$C_k (V_{dd} + V_{k-1}) - \Delta Q_{i2k} = C_k V_k. \tag{28}$$

Using (11) and that E_{i2k} is equal to $V_{dd}\Delta Q_{i2k}$, we have

$$E_{i2k} = \frac{1}{1+\alpha} (V_{dd} I_o T + \alpha C_k V_{dd}^2). \tag{29}$$

Special care is needed for C_N, as its discharging phase consists of two parts. The first part is for C_N to redistribute charge with C_L, and the charge supplied by V_{dd} is ΔQ_{i2N1}:

$$C_N (V_{dd} + V_{N-1}) - \Delta Q_{i2N1} = C_N (V_{o1} - V_{dd}). \tag{30}$$

The second part is discharging C_N and C_L by I_o for half of the period, and the charge supplied by V_{dd} to C_N is ΔQ_{i2N2}:

$$C_N(V_{o1} - V_{dd}) - \Delta Q_{i2N2} = C_N(V_{o2} - V_{dd}) . \tag{31}$$

Using (7) in (31), and that the total cycle energy E_{i2N} is given by $V_{dd}(\Delta Q_{i2N1}+\Delta Q_{i2N2})$, we have

$$E_{i2N} = \frac{1}{1+\alpha}(V_{dd}I_oT + \alpha C_N V_{dd}^2) . \tag{32}$$

Here we proved that E_{i2N} is independent of C_L and has the same form as E_{i2k}. For the negative-plate parasitic capacitors, it is easy to obtain E_{i3k} as

$$E_{i3k} = \beta C_k V_{dd}^2 . \tag{33}$$

From Section 3, the optimal capacitor assignment is C_k=C. Therefore, in combining (27), (29), (32) and (33) we have

$$\eta = \frac{V_oI_oT}{\left(1+\frac{N}{1+\alpha}\right)V_{dd}I_oT + \frac{\alpha}{1+\alpha}NCV_{dd}^2 + \beta NCV_{dd}^2} . \tag{34}$$

From the above discussion, we observe that the input cycle energy E_i is independent of C_L. In fact, C_L plays an important role in determining the output voltage ripple (5), but has a negligible effect on the average output voltage (16). For all practical purposes, we may assume C_L=∞, and (34) can be written as

$$\eta = \frac{N+1+\alpha-N\delta}{N+1+\alpha+\frac{N(\alpha+\beta+\alpha\beta)}{\delta}} . \tag{35}$$

The reduction factor δ is required to be small if the output voltage has to be as large as possible, for example, δ<0.05. However, a small δ is achieved by a large C, which translates to large losses of αCV_{dd}^2 and βCV_{dd}^2. From (35), both the positive-plate and negative-plate parasitic capacitors have comparable effect on the efficiency. To maximize efficiency, if N is fixed, the only parameter that can be changed is δ, and we need to solve for the condition dη/dδ=0. To make the differentiation easier, we rewrite (35) as

$$\eta = \frac{\delta(1-\mu\delta)}{(\mu\lambda+\delta)} , \tag{36}$$

with

$$\mu = \frac{N}{N+1+\alpha} , \tag{37}$$

$$\lambda = \alpha+\beta+\alpha\beta . \tag{38}$$

The optimal reduction factor is obtained as

$$\delta_{opt} = \mu\lambda\left(\sqrt{1+\frac{1}{\mu^2\lambda}}-1\right), \tag{39}$$

and the corresponding maximum efficiency is

$$\eta_{max} = 1-2\mu\delta_{opt}\,. \tag{40}$$

However, if a predefined V_o has to be achieved, δ_{opt} obtained in (39) may not satisfy (22). To satisfy (22), we substitute

$$\delta = \frac{N+1+\alpha-(1+\alpha)M}{N} \tag{41}$$

into (35) and obtain

$$\eta = \frac{(1+\alpha)M}{N+1+\alpha+\dfrac{\lambda N^2}{N-(1+\alpha)(M-1)}}\,. \tag{42}$$

As $(1+\alpha)M$ is a constant, maximizing η is the same as minimizing the denominator:

$$\gamma = N+1+\alpha+\frac{\lambda N^2}{N-(1+\alpha)(M-1)}\,, \tag{43}$$

and $d\gamma/dN=0$ is satisfied if

$$N_{opt} = (1+\alpha)\left(1+\sqrt{\frac{\lambda}{1+\lambda}}\right)(M-1)\,. \tag{44}$$

Note that if $\alpha=0$, then (44) is reduced to

$$N_{opt}\big|_{\alpha=0} = \left(1+\sqrt{\frac{\beta}{1+\beta}}\right)(M-1) \tag{45}$$

which gives the same result as obtained in [5]. The design strategy according to the above analysis will be discussed in details in Section 10.

5 Analysis of Dual-Branch Linear Charge Pumps

Dual-branch and multi-phase charge pumps result in smaller output voltage ripples than single-branch counterparts, and in-depth analysis is needed to obtain the design equations [13, 16]. Fig. 5 shows the schematic of a dual-branch (N+1)X linear charge pump, with the two branches operating in complementary phases. Only the charging and discharging phases of Branch A are labeled. Due to symmetry, we assign

C_{Ak}=C_{Bk}=C_k, but we still use C_{Ak} and C_{Bk} when clarity in description is needed. Negative-plate parasitic capacitors are not shown. Fig. 6 shows the timing diagrams of C_N and $V_o(t)$, as those of C_1 and C_k are the same as the single-branch case.

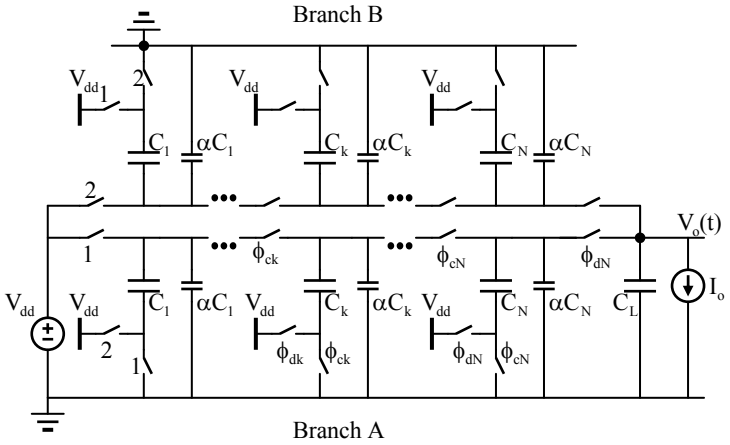


Fig. 5. Dual-branch (N+1)X linear charge pump.

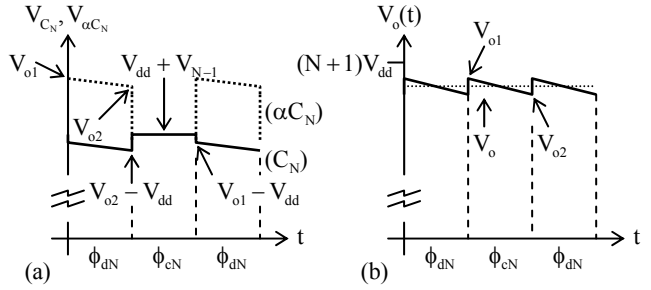


Fig. 6. Timing diagram of dual-branch LQP of (a) C_N; and (b) $V_o(t)$.

The analysis follows closely that of the single-branch case and is skipped. The key results of V_{o1}, V_{o2} and the average output voltage V_o=(V_{o1}+V_{o2})/2 are shown below:

$$V_{o1} = \frac{N+1+\alpha}{1+\alpha} V_{dd} - \sum_{k=1}^{N} \frac{I_o T/2}{(1+\alpha)C_k} + \frac{I_o T/2}{(1+\alpha)C_N + C_L}, \tag{46}$$

$$V_{o2} = \frac{N+1+\alpha}{1+\alpha} V_{dd} - \sum_{k=1}^{N} \frac{I_o T/2}{(1+\alpha)C_k}, \tag{47}$$

$$V_o = \frac{N+1+\alpha}{1+\alpha} V_{dd} - \sum_{k=1}^{N} \frac{I_o T/2}{(1+\alpha)C_k} + \frac{I_o T/4}{(1+\alpha)C_N + C_L}. \tag{48}$$

Note again that V_{o2} is independent of C_L. For C_L>>C_k, the average output voltage V_o is equal to V_{o2}, and to maximize V_{o2} and minimize the total capacitance C_T it is clear that all C_k should be set equal:

$$C_1 = C_2 = ... = C_N = C_{II}, \tag{49}$$

where the subscript II is for the dual-branch case. The output voltage with C_L>>C_k is

$$V_o = \frac{N+1+\alpha}{1+\alpha} V_{dd} - \frac{NI_oT/2}{(1+\alpha)C_{II}}, \tag{50}$$

and the output voltage ripple by restating a finite C_L (>>C_k) is

$$\Delta V_o = \frac{I_oT}{2C_L}. \tag{51}$$

As in Section 3, if we assign the reduction factor δ_{II} as

$$\delta_{II} = \frac{I_oT}{C_{II}V_{dd}} = \frac{I_oT}{(C/2)V_{dd}} = 2\delta, \tag{52}$$

then the voltage conversion ratio is

$$M_{II} = \frac{V_o}{V_{dd}} = \frac{N+1+\alpha-N\delta_{II}/2}{1+\alpha}. \tag{53}$$

Compare (50) and (19), if we assign

$$C_{II} = C/2 \tag{54}$$

then both single-branch and dual-branch charge pumps have the same output voltage V_o for the same total capacitance C_T (note that $2NC_{II}$=NC for the dual-branch LQP). The only difference between the two LQPs is the output voltage ripple, with the dual-branch LQP being only half of that of the single-branch case. The equation for efficiency of the dual-branch LQP is the same as (35) by replacing δ with $\delta_{II}/2$, and therefore, all equations (36) through (45) apply to both the single-branch and dual-branch linear charge pumps.

6 Comparison of Single- and Dual-Branch Linear Charge Pumps

We validate the analyses of single- and dual-branch linear charge pumps for the following aspects. (A) Perform time-domain Cadence simulation to verify equations (5, 13-15) of the single-branch LQP, and equations (46-48) of the dual-branch LQP. (B) Perform Cadence simulations on output voltage and efficiency of (A) and compare with theoretical results. (C) Perform Matlab simulation of δ_{opt} and η_{max} for different N, α and β. Cadence simulations will be performed and compared with theoretical values. For all Cadence simulations presented in this paper, the switches

are realized by nearly ideal switches that have very low on-resistance of 0.1Ω and very large off-resistance of 1TΩ. Simulations are performed using relative tolerance of 10^{-6}, absolute tolerance in current of 1pA, and absolute tolerance in voltage of 1μV.

(A) For time-domain simulation, we design single-branch and dual-branch 8X LQPs (N=7) with the following specification: the input voltage V_{dd} is 1V, the load current I_o is 10μA, and the switching frequency f_s is 10MHz. The positive-plate and negative-plate parameters are α=0.01 and β=0.05, respectively. The non-overlapping dead time is set to be 1ns.

For the single-branch 8X LQP, we set C=20pF and C_L=25pF. Fig. 7(a) shows the simulation result of $V_o(t)$ on which V_{o1}, V_{o2} and V_{o3} are marked. For the dual-branch 8X LQP, we set C_{II}=10pF and C_L=25pF. Fig. 7(b) shows the simulation result of $V_o(t)$ on which V_{o1} and V_{o2} are marked. Table 1 tabulates the analysis and simulation results along with the percentage errors. The errors for V_{oi}'s are due to the switch dead time in our simulation and are all smaller than 0.013%.

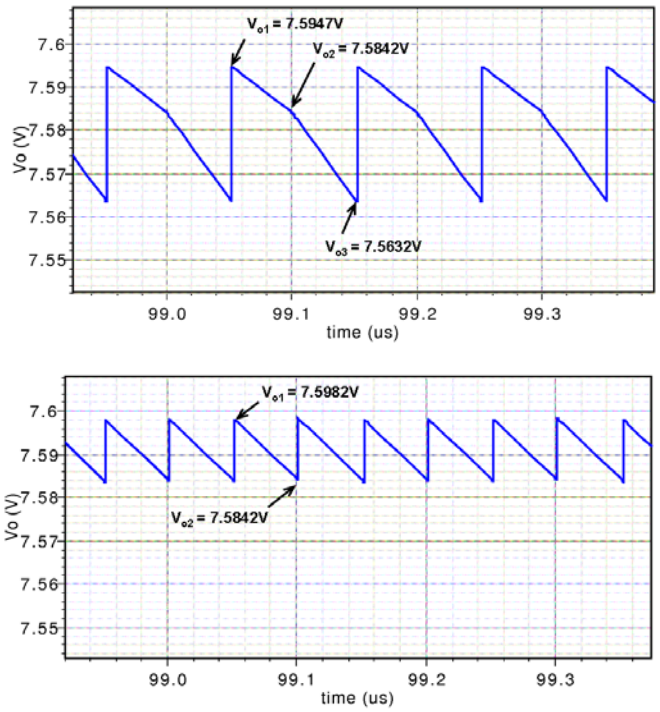


Fig. 7. Time-domain simulation of (a) single-branch LQP; and (b) dual-branch LQP.

(B) The reduction factors of the charge pumps in (A) are δ=0.05 and δ_{II}=0.1, respectively, and are not the optimal values. Efficiency computations are performed for C_L=25pF and C_L=1nF (such that it can be regarded as infinite), and both are only

around 46.5% (Table 2). Next, for the single-branch charge pump with N=7, α=0.01, β=0.05 and C_L=1nF, δ_{opt} is computed from (39) to be 0.1987 and η_{max} is 65.27%. Cadence simulation gives an almost identical efficiency of 65.29%. The results are again tabulated in Table 2.

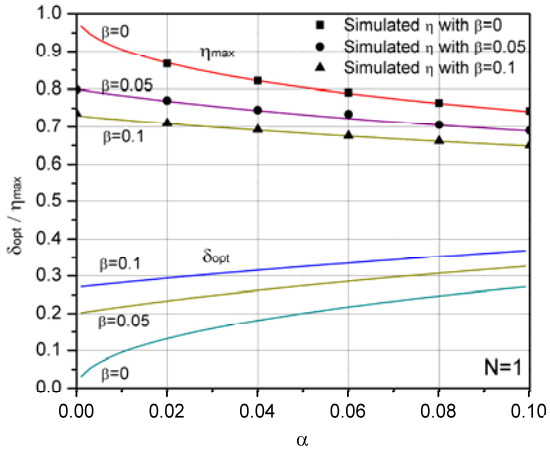
(C) We would like to find out the general range of δ_{opt} and the corresponding η_{max}. Fig. 8 shows δ_{opt} and η_{max} vs α, β and N. The negative-plate parasitic parameter β takes the value of 0.00, 0.05 and 0.10, while the positive-plate parasitic parameter α ranges from 0.00 to 0.10 for N=1 (voltage doubler), N=3 and N=7. Cadence simulations are also performed for α=0 to α=0.10 at an interval of 0.02. The theoretical curves match very well with Cadence simulations.

Table 1. Output voltages and output voltage ripples of LQPs.

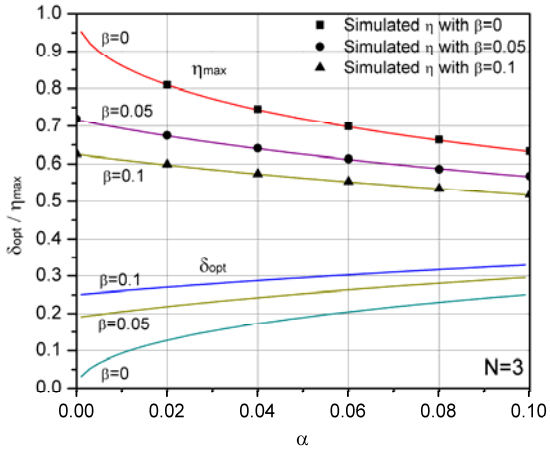
	Analysis	**Simulation**	**% error**
Single-branch			
V_{o1}	7.5952V	7.59470V	0.006%
V_{o2}	7.5842V	7.58419V	0.0001%
V_{o3}	7.5642V	7.56319V	0.013%
ΔV_o	31.1mV	31.5mV	1.29%
Dual-branch			
V_{o1}	7.5984V	7.5982V	0.0026%
V_{o2}	7.5842V	7.5835V	0.0092%
ΔV_o	14.2mV	14.7mV	3.52%

Table 2. Output voltages and efficiencies of LQPs.

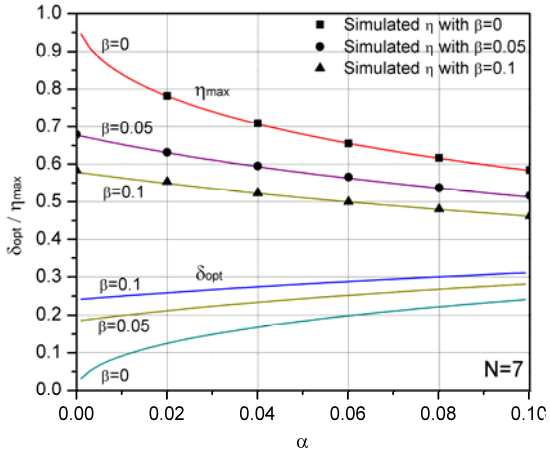
	Analysis	**Simulation**	**% error**
Single-branch with δ=0.05, C=20pF, C_L=25pF			
V_o	7.5820V	7.5816V	0.0053%
η	46.47%	46.49%	0.043%
Single-branch with δ=0.05, C=20pF, C_L=1nF			
V_o	7.5842V	7.5841V	0.0013%
η	46.48%	46.51%	0.065%
Dual-branch with δ_{II}=0.1, C_{II}=10pF, C_L=25pF			
V_o	7.5913V	7.5909V	0.0053%
η	46.52%	46.54%	0.043%
Dual-branch with δ_{II}=0.1, C_{II}=10pF, C_L=1nF			
V_o	7.5844V	7.5843V	0.0013%
η	46.48%	46.50%	0.043%
Single-branch with δ_{opt}=0.1987, C=5.032pF, C_L=1nF			
V_o	6.5535V	6.5534V	0.0015%
η	65.27%	65.29%	0.031%



(a)



(b)



(c)

Fig. 8. δ_{opt} and η_{max} for (a) N=1; (b) N=3; and (c) N=7.

7 Analysis of Fibonacci Charge Pumps

Fig. 9 shows a single-branch 8X Fibonacci charge pump, leaving out all parasitic capacitors for a clear exposition of the topology [9]. It uses only four flying capacitors to achieve a voltage conversion ratio of 8. An immediate question is: will the total capacitance be smaller than that of the 8X LQP for the same output voltage V_o? In fact, the same question can be asked of the 8X exponential charge pump to be discussed in Section 8. For a complete analysis with $C_L \neq 0$ including parasitic capacitors, it can be shown, by following the procedure as discussed in Section 3, that V_{o2} of both single- and dual-branch charge pumps are independent of C_L, and as $C_L \to \infty$, $V_o \to V_{o2}$. Therefore, we assume $C_L = \infty$ to arrive at a simpler procedure as discussed below.

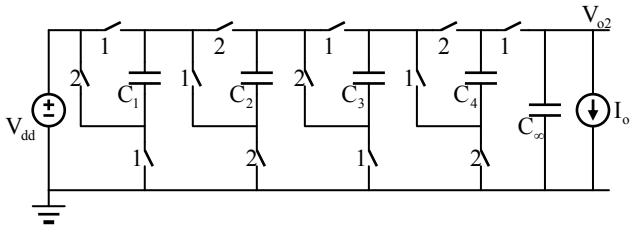


Fig. 9. Single-branch 8X Fibonacci charge pump.

Fig. 10 shows the connections of the switches, the flying capacitors and their parasitic capacitors of the 8X FQP in both $\phi_1=1$ and $\phi_2=1$. As discussed in Section 3, for any flying capacitor C_k, the charging phase is ϕ_{ck} and the discharging phase is ϕ_{dk}, and the capacitor voltage when fully discharged in $\phi_{dk}=1$ is designated as V_k. Clearly, in $\phi_{c1}=\phi_1=1$, C_1 is charged to V_{dd}, and in $\phi_{d1}=\phi_2=1$, C_1 is discharged to V_1, but then ϕ_{d1} is the same as ϕ_{c2}, and C_2 is charged to $V_{dd}+V_1$. The same mechanism propagates down the stages, and it also applies to the parasitic capacitors. Let us consider the case with $\alpha=\beta=0$ first. It is straightforward to work from the last stage back to the first stage. In the charging phase of C_4 (i.e., $\phi_2=1$), C_4 is charged to $V_{dd}+V_1+V_3$, while C_∞ is discharged by I_o for the duration of T/2. In the discharging phase, C_4 is stacked on top of V_{dd} and C_2, and C_4 supports I_o for T/2, and C_4 is eventually discharged to V_4. Employ QBL, we have

$$C_4(V_{dd} + V_1 + V_3) = C_4V_4 + I_oT\,. \tag{55}$$

Note that for $C_L=C_\infty=\infty$, the output voltage V_{o2} will never change, and we need to account for the load current consumption as discussed above so that the result would be correct. Next, for charge transfer at V_d ($\phi_1 \to \phi_2$), we have

$$C_3(V_{dd} + V_2) + C_4V_4 = C_3V_3 + C_4(V_{dd} + V_1 + V_3)\,, \tag{56}$$

and it can be simplified using the result of (55) to give

$$C_3(V_{dd} + V_2) = C_3V_3 + I_oT\,. \tag{57}$$

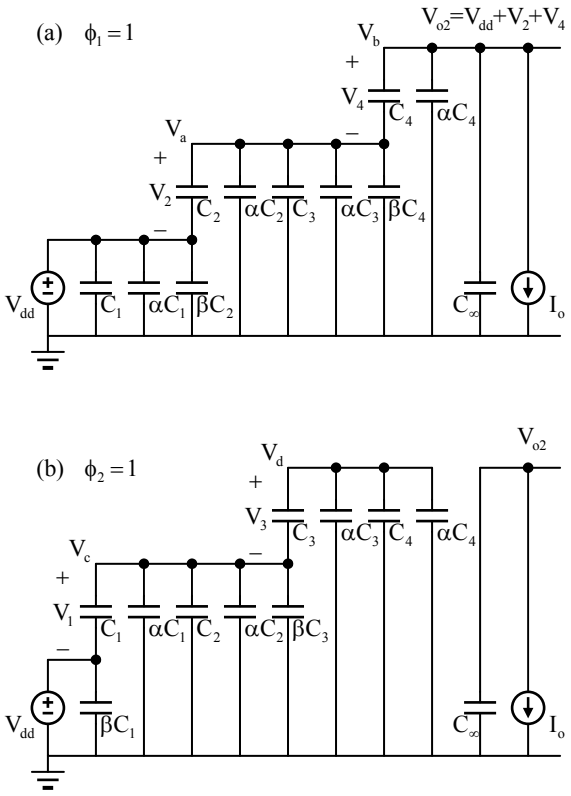


Fig. 10. Capacitor connections of 8X FQP in (a) ϕ_1=1; and (b) ϕ_2=1.

The charge transfer at V_a ($\phi_2 \rightarrow \phi_1$) is not as straightforward, as it is the negative plate of C_4 that is connected to V_a. Taking this into consideration and we obtain

$$C_2(V_{dd} + V_1) + C_3V_3 - C_4(V_{dd} + V_1 + V_3) = C_2V_2 + C_3(V_{dd} + V_2) - C_4V_4 . \tag{58}$$

Using both (55) and (57) gives

$$C_2(V_{dd} + V_1) = C_2V_2 + I_oT . \tag{59}$$

In a similar fashion, the charge transfer at V_c ($\phi_1 \rightarrow \phi_2$) gives

$$C_1V_{dd} = C_1V_1 + 3I_oT . \tag{60}$$

Backward substitution can then be performed, and we obtain

$$V_1 = V_{dd} - \frac{3I_oT}{C_1} , \tag{61}$$

$$V_2 = 2V_{dd} - \frac{3I_oT}{C_1} - \frac{2I_oT}{C_2}, \tag{62}$$

$$V_3 = 3V_{dd} - \frac{3I_oT}{C_1} - \frac{2I_oT}{C_2} - \frac{I_oT}{C_3}, \tag{63}$$

$$V_4 = 5V_{dd} - \frac{3I_oT}{C_1} - \frac{2I_oT}{C_2} - \frac{I_oT}{C_3} - \frac{I_oT}{C_4}. \tag{64}$$

Finally, $V_{o2} = V_{dd}+V_2+V_4$, and we have

$$V_{o2} = 8V_{dd} - \frac{9I_oT}{C_1} - \frac{4I_oT}{C_2} - \frac{I_oT}{C_3} - \frac{I_oT}{C_4}. \tag{65}$$

The analysis of a higher order FQP is similar, and one can easily infer the result from observing the above trend of V_k. From (65), it is obvious that the capacitors should not have the same value: the $1/C_1$ term has a weight of 9, the $1/C_2$ term has a weight of 4, and the $1/C_3$ and $1/C_4$ terms have weights of 1. Qualitatively, C_1 should be larger to minimize the reduction due to a larger weight. Quantitatively, to minimize the total capacitance, the procedure described in [1, 13] should be followed, and the optimal assignment is

$$C_1 = 3C, \tag{66}$$

$$C_2 = 2C, \tag{67}$$

$$C_3 = C_4 = C, \tag{68}$$

$$C_T = C_1 + C_2 + C_3 + C_4 = 7C. \tag{69}$$

Using the above optimal assignment for the ideal case, we have

$$V_{o2} = 8V_{dd} - \frac{7I_oT}{C}. \tag{70}$$

This is the same result as obtained for the single-branch 8X LQP with α=0 (19). Therefore, for on-chip implementation, there is no advantage in saving capacitor area by using FQP instead of LQP. This is a very important conclusion of this research. Nevertheless, we continue to work out the voltage conversion ratio in the presence of αC_k and βC_k, as the result would be useful for off-chip implementation.

In analyzing FQP including αC_k and βC_k, we propose a **first iteration approximation** (FIA) analysis. This procedure can work with both αC_k and βC_k together, but for the purpose of illustration, let us consider only αC_k first (β=0). Again, we consider the charge transfer at V_b ($\phi_2 \rightarrow \phi_1$) and obtain

$$(1+\alpha)C_4(V_{dd}+V_1+V_3)=C_4V_4+\alpha C_4(V_{dd}+V_2+V_4)+I_oT\,. \tag{71}$$

Eq. (71) can be rearranged to read

$$C_4(V_{dd}+V_1+V_3)=C_4V_4+\alpha C_4(V_4-V_3+V_2-V_1)+I_oT\,. \tag{72}$$

Following the same procedure and rearranging the corresponding equations as in (72), we have

$$C_3(V_{dd}+V_2)=C_3V_3+\alpha C_3(V_3-V_2+V_1)+I_oT\,, \tag{73}$$

$$C_2(V_{dd}+V_1)=C_2V_2+\alpha C_2(V_2-V_1)+\alpha C_4(V_4-V_3+V_2-V_1)+2I_oT\,, \tag{74}$$

$$C_1V_{dd}=C_1V_1+\alpha C_1V_1+\alpha C_3(V_3-V_2+V_1)+\alpha C_4(V_4-V_3+V_2-V_1)+3I_oT\,. \tag{75}$$

The difficulty of solving (72) to (75) lies with the parasitic terms αC_k. Consider (72). If α is very small, the term with αC_4 should be much smaller than the terms with C_4 only. If there is an error in the multiplicand of αC_4 (that is, $V_4–V_3+V_2–V_1$), the error would be of second order and can be neglected. Now, for $\alpha,\beta,\delta << 1$, we have $V_4\approx 5V_{dd}$, $V_3\approx 3V_{dd}$, $V_2\approx 2V_{dd}$ and $V_1\approx V_{dd}$. Using this approximation we have

$$\alpha C_4(V_4-V_3+V_2-V_1)\approx 3\alpha C_4V_{dd}\,. \tag{76}$$

Performing the same approximation for (73), (74) and (75) by also including $\beta\neq 0$ we obtain

$$V_1\approx V_{dd}-\frac{8\alpha}{3}V_{dd}-\frac{5\beta}{3}V_{dd}-\frac{I_oT}{C}\,, \tag{77}$$

$$V_2\approx 2V_{dd}-\frac{31\alpha}{6}V_{dd}-\frac{19\beta}{6}V_{dd}-\frac{2I_oT}{C}\,, \tag{78}$$

$$V_3\approx 3V_{dd}-\frac{43\alpha}{6}V_{dd}-\frac{19\beta}{6}V_{dd}-\frac{3I_oT}{C}\,, \tag{79}$$

$$V_4\approx 5V_{dd}-\frac{77\alpha}{6}V_{dd}-\frac{29\beta}{6}V_{dd}-\frac{5I_oT}{C}\,, \tag{80}$$

$$V_{o2(FQP)}\approx 8V_{dd}-18\alpha V_{dd}-8\beta V_{dd}-\frac{7I_oT}{C}\,. \tag{81}$$

This output voltage is much lower than that of the LQP (19):

$$V_{o2(LQP)}\approx 8V_{dd}-7\alpha V_{dd}-\frac{7I_oT}{C}\,. \tag{82}$$

Clearly, linear charge pumps are preferred to Fibonacci charge pumps for on-chip implementation.

8 Analysis of Exponential Charge Pumps

Fig. 11 shows the dual-branch exponential charge pump that uses 2N flying capacitors and one load capacitor [10, 11]. Note that with N flying capacitors, a 2^NX charge pump can only be realized using a multi-phase clock [17, 18]. The analysis is left as a challenge to the readers and only the key results are presented below. For the optimal capacitor assignment with $\alpha=\beta=0$, we have

$$C_{1A} = C_{1B} = 4C_{II}, \tag{83}$$

$$C_{2A} = C_{2B} = 2C_{II}, \tag{84}$$

$$C_{3A} = C_{3B} = C_{II}, \tag{85}$$

$$C_T = 2\times(C_{1A} + C_{2A} + C_{3A}) = 14C_{II}. \tag{86}$$

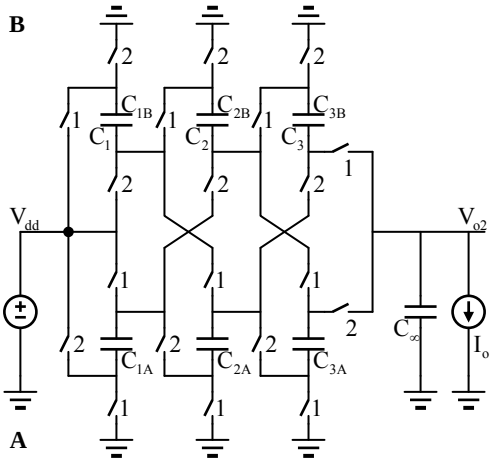


Fig. 11. Dual-branch 8X exponential charge pump.

For $\alpha,\beta \neq 0$, we use first iteration approximation and the final capacitor voltages V_k and V_{o2} are

$$V_1 \approx V_{dd} - 4\alpha V_{dd} - 3\beta V_{dd} - \frac{I_o T}{2C_{II}}, \tag{87}$$

$$V_2 \approx 2V_{dd} - 8\alpha V_{dd} - 5\beta V_{dd} - \frac{I_o T}{C_{II}}, \tag{88}$$

$$V_3 \approx 4V_{dd} - 16\alpha V_{dd} - 8\beta V_{dd} - \frac{2I_o T}{C_{II}}, \tag{89}$$

$$V_{o2(EQP)} \approx 8V_{dd} - 28\alpha V_{dd} - 16\beta V_{dd} - \frac{7I_oT}{2C_{II}}. \quad (90)$$

This result is to be compared with (81) and (82) for $\alpha=\beta=0$: with $C_{II}=C/2$, all LQP, FQP and EQP have the same output voltage using the same total capacitance. For the same $\alpha\neq0$ and/or $\beta\neq0$, LQP achieves the highest voltage conversion ratio, and EQP achieves the lowest voltage conversion ratio.

9 Comparison of LQPs, FQPs and EQPs

For the purpose of comparison, we design single-branch 8X LQP and 8X FQP, and dual-branch 8X LPQ, 8X FQP and 8X EQP with the following specification: the input voltage V_{dd} is 1V, the load current I_o is 10μA, and the switching frequency f_s is 10MHz. Ideal switches are used and the non-overlapping dead time is set to be 1ns. The single-branch unit capacitor $C_{(1B)}=C$ is 20pF, such that the reduction factor $\delta = I_oT/(CV_{dd})$ is 0.05, and the total capacitance of all charge pumps are $C_T=140$pF. The load capacitor C_L is 1nF to fulfill the assumption of $C_L>>C_k$. Due to limited space, only the time-domain simulation of the single-branch 8X FQP is shown. Fig. 12 shows the positive-plate voltages of C_k and the output voltage $V_o(t)$ for the case with $\alpha=0.025$ and $\beta=0.04$. As $C_L\neq\infty$, $V_o(t)$ is not a constant; but the mid-voltage of $V_o(t)$ is V_{o2} as shown.

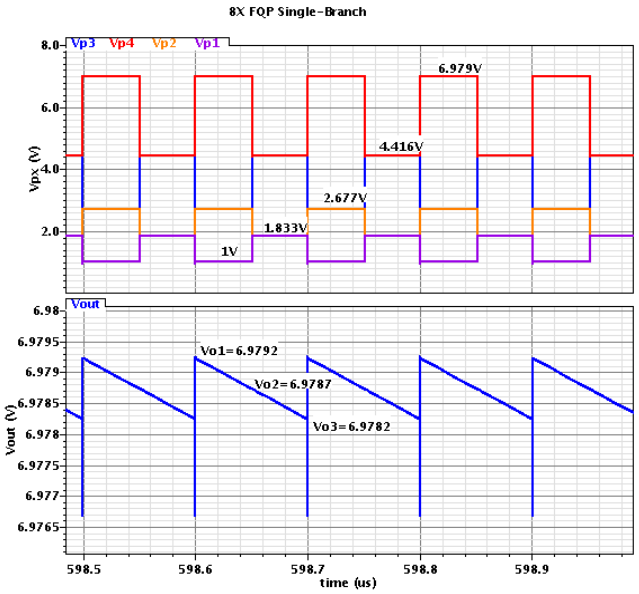


Fig. 12. Simulated waveforms of single-branch 8X FQP.

The simulated values are to be compared with the computed values using FIA analysis. Consider the positive-plate voltage of C_4. The maximum value (in the discharging phase) is 6.979V, and the minimum value (in the charging phase) is 2.677V. Hence, $V_{4(sim)}$ = 6.979–2.677 = 4.302V. The curves are a little bit difficult to read due to overlapping. Eq. (81) gives $V_{4(comp)}$ = 4.236V, and the error is –1.6%. The computed and simulated values are compiled in Table 3. Note that in FIA analysis, V_k in the αC_k terms are over-estimated, and they lead to consistently under estimation of the computed V_k terms.

Fig. 13 shows the time-domain simulation of the dual-branch 8X FQP with $C_{(2B)}$= C_{II}=C/2=10pF, such that C_T=140pF. Except for the reduction in output voltage ripple as discussed in [13], the corresponding voltages of the dual-branch FQP are the same as the single-branch counterpart, verifying our conclusion that they should have the same performance when C_L=∞.

The second set of simulations is to plot the output voltage V_{o2} vs α and V_{o2} vs β individually. Here, all three charge pumps are dual-branch charge pumps. Optimal capacitance assignment for the respective ideal case is used. Hence, for the 8X LQP, $C_{kA} = C_{kB} = C$ = 10pF, where the subscript "A" is for the A-branch, and "B" for the B-branch. For the 8X FQP, C_{1A}:C_{2A}:C_{3A}:C_{4A} = C_{1B}:C_{2B}:C_{3B}:C_{4B} = 3C:2C:C:C; and for the 8X EQP, C_{1A}:C_{2A}:C_{3A} = C_{1B}:C_{2B}:C_{3B} = 4C:2C:C. For all three charge pumps, the total on-chip capacitance C_T is 140pF, and C_L = 1nF.

Fig. 14 shows the simulation results of V_{o2} vs α and V_{o2} vs β for all three charge pumps, with both α and β changed from 0 to 0.1. The calculated results match the simulated results quite well when α and β are small, as shown in Table 3: for α=0.025 and β=0.04, the error is only -1.4%. The differences become larger for larger α and β. To enhance the accuracy in computation, a more complicated second iteration approximation has to be used.

Table 3. Computed and Simulated values of 8X FQP.

	Computed	**Simulated**	**Error**
V_1	0.817V	1.833 - 1.000 = 0.833V	-2.0%
V_2	1.644V	2.677 - 1.000 = 1.677V	-2.0%
V_3	2.544V	4.416 - 1.833 = 2.583V	-1.5%
V_4	4.236V	6.979 - 2.677 = 4.302V	-1.6%
V_{o2}	6.880V	6.979V	-1.4%

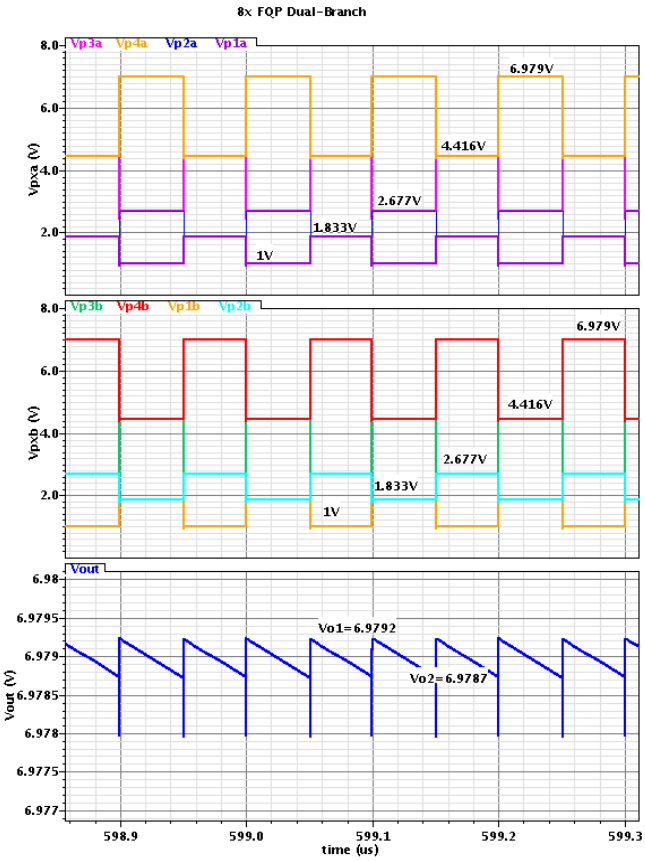
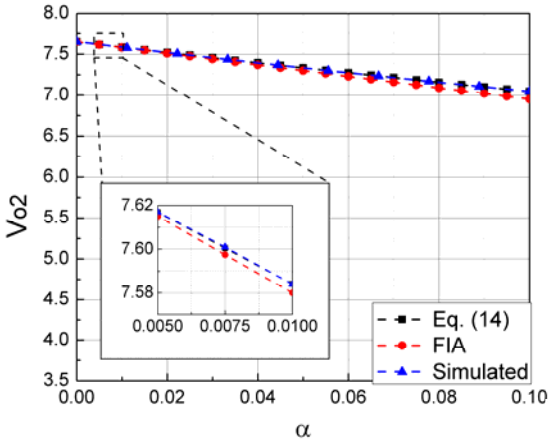
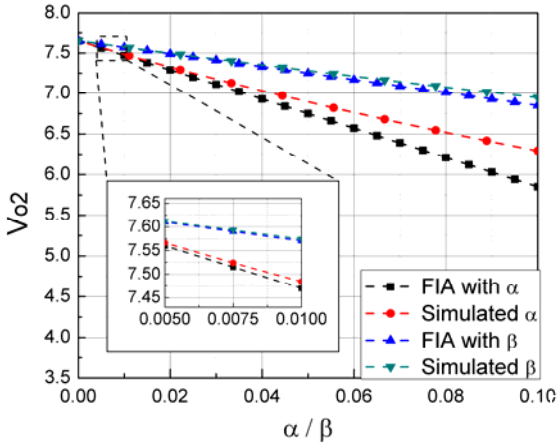


Fig. 13. Simulated waveforms of dual branch 8X FQP.



(a)



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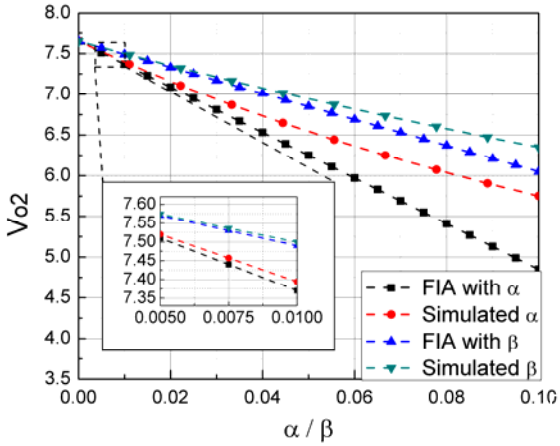

(c)

Fig. 14. V_{o2} vs α and V_{o2} vs β for (a) LQP; (b) FQP; and (c) EQP.

10 Design Strategy of Optimal Linear Charge Pumps

As the linear charge pump is the most efficient on-chip implementation, it is worthwhile to devise a design strategy in optimizing the efficiency for a specified output voltage. Table 4 summarizes the design strategies proposed in [5] and [6], along with our own proposal. The design strategy of [5] has been very successful in optimizing the efficiencies of LQPs and worth repeating in some details. In [5], instead of working directly on η, the input current I_{in} consisting of the currents

flowing into the negative-plate parasitic capacitors βC_k were used to find N_{opt} that minimizes I_{in}, while αC_k were left out. In assuming $\alpha=0$, N_{opt} is computed using (45). The input current I_{in} with $\alpha=0$ is derived as [5]

$$I_{in}\big|_{\alpha=0} = \left(N+1+\frac{\beta N^2}{N+1-M} \right) I_o \,. \tag{91}$$

Then the flying capacitor C is computed using (21) and (41), and η can be obtained from (35), all with $\alpha=0$ (Table 4).

The drawback of [5] is in neglecting αC_k. In present-day technology, an MIM (metal-insulator-metal) capacitor has a capacitance of 1fF/μm^2. The bottom-plate (usually implemented as negative-plate) parasitic parameter is β=0.01~0.05, while the top-plate (usually implemented as positive-plate) parasitic parameter is 0.1fF/μm of perimeter. If the unit capacitor is 1.6pF, it could be realized by a 40μm×40μm MIM capacitor, and α=0.01. If the unit capacitor is 400fF, then α increases to 0.02. Moreover, when switches or diodes are taken into consideration, additional parasitic capacitors will be added to both plates. Therefore, the assumption that αC_k are negligible may not be justified.

Table 4. Comparison of analyses and optimization methods of LQPs.

	[5]	**[6]**	**This work**
	$\alpha = 0,\ \beta \neq 0$	$\alpha \neq 0,\ \beta \neq 0$	$\lambda = \alpha+\beta+\alpha\beta$
N_{opt}	$\left(1+\sqrt{\frac{\beta}{1+\beta}}\right)(M-1)$	N is given a priori	$(1+\alpha)\left(1+\sqrt{\frac{\lambda}{1+\lambda}}\right)(M-1)$
$\delta = \frac{I_o T}{C V_{dd}}$	$\frac{N+1-M}{N}$	C is given a priori	$\frac{N+1+\alpha-(1+\alpha)M}{N}$
V_o	$(N+1)V_{dd} - \frac{NI_oT}{C}$	$\frac{N+1+\alpha}{1+\alpha} V_{dd} - \frac{NI_oT}{(1+\alpha)C}$	$\frac{N+1+\alpha}{1+\alpha} V_{dd} - \frac{NI_oT}{(1+\alpha)C}$
η	$\frac{M}{N+1+\frac{N\beta}{\delta}}$	$\frac{M}{N+1+\frac{(2N+1)\alpha}{1+\alpha}+\frac{N\beta}{\delta}}$	$\frac{(1+\alpha)M}{N+1+\alpha+\frac{N(\alpha+\beta+\alpha\beta)}{\delta}}$

An attempted to perfect the analysis of [5] by including the input currents of αC_k was proposed in [6]. Ref. [6] did not show how N is computed, and it is reasonable to use N_{opt} and δ as computed in [5]. By using the formula for V_o due to [2] that includes αC_k, V_o was accurately estimated (Table 4). However, all αC_k were assumed to be charged in both phases (that gives the factor 2N+1 shown in Table 4) and was thus not accurate enough. Moreover, the parameter $V_{C/D}$ in [6] was not derived correctly.

Our proposed design strategy complements that of [5] by correctly accounting for the effects of αC_k. By grouping the denominator of (34) as $V_{dd}I_{in}T$, the input current I_{in} is obtained as

$$I_{in} = \left(N + 1 + \alpha + \frac{(\alpha + \beta + \alpha\beta)N^2}{N + 1 + \alpha - (1+\alpha)M} \right) \frac{I_o}{1+\alpha} . \tag{92}$$

The dependence of α in (92) cannot be obtained very easily through ad hoc addition of αC_k terms to (91), but it can be handled correctly through using the systematic application of the charge balance law as shown in Section 4. It is obvious that minimizing I_{in} of (92) is the same as minimizing γ of (43).

Following the steps in [5], N_{opt} is first computed using (44) that correctly accounts for αC_k (Table 4). From Fig. 14, it is clear that η_{max} decreases as N increases for the same α and β. Qualitatively, using a larger N to realize the same output conversion ratio M means that more C_k have to be used, and there will be more losses from αC_k and βC_k. Therefore, a smaller N is preferred if the realized V_o is acceptable for that application. After N is determined, one then has two choices in computing C: the first one is to compute C using (39), such that maximum efficiency is guaranteed, but the realized output voltage may deviate from the required V_o; and the second one is to compute C using (41) such that $V_o = MV_{dd}$ as required. Here, we propose that we should compute C using (41) whatsoever to make sure that the realized output voltage is the same as the specification, while the degradation in efficiency is too small to be of concern. Our argument is as follow. When δ is not equal to δ_{opt}, the efficiency η can be obtained from η_{max} using Taylor's series expansion:

$$\eta = \eta_{max} + \left.\frac{d\eta}{d\delta}\right|_{\delta_{opt}} \Delta\delta + \frac{1}{2}\left.\frac{d^2\eta}{d\delta^2}\right|_{\delta_{opt}} \Delta\delta^2 + \cdots . \tag{93}$$

The maximum efficiency is obtained by finding the condition for $d\eta/d\delta=0$; hence, the first order term is zero. For the second derivative, it can easily be shown that

$$\left.\frac{d^2\eta}{d\delta^2}\right|_{\delta_{opt}} = \frac{-2\mu}{\mu\lambda + \delta_{opt}} . \tag{94}$$

giving

$$\eta \approx \eta_{max} - \mu \left(1 - \frac{1}{\sqrt{1 + \frac{1}{\mu^2\lambda}}} \right) \left(\frac{\Delta\delta}{\delta_{opt}} \right)^2 . \tag{95}$$

In general, the coefficient of the $(\Delta\delta/\delta_{opt})^2$ term is smaller than unity. For $\Delta\delta/\delta_{opt} = \pm 0.1$ (10% deviate from the optimal value), the decrease in efficiency is only less than 1%. Hence, we conclude that C should be computed using (41).

As an example, let us design a charge pump that has an average output voltage V_o of 5V (M=5) with the following specifications: the input voltage V_{dd} is 1V, the load current I_o is 10μA, and the switching frequency f_s is 10MHz. The positive-plate and negative-plate parameters are α=0.01 and β=0.06, respectively. The load capacitor is C_L=1nF.

For the design according to [5], N_{opt} and δ are computed using the corresponding formulae in Table 4. N_{opt} is computed to be 4.95, and naturally N is taken as 5. As α is assumed to be zero while actually it is 0.01, both the output voltage V_o and the efficiency η are overestimated, as the simulation results in Table 5 show.

For the design according to [6], N_{opt} and δ are obtained as in [5]. As the accurate formula for V_o is used, the theoretical value (4.9604V) is very close to the simulated value (4.960V). Moreover, as the effects of αC_k are partially accounted for, the theoretical efficiency (0.6519) is closer to the simulated value (0.6466) than that of [5] (0.6667).

For our proposed design, N_{opt} is computed using (44), and the value is 5.08. We choose N=5 instead of N=6 because it is closer to 5.08, and we can use (41) to compute δ that still satisfies M=5. The reduction factor δ is computed to be 0.192. Both the theoretical and the simulation values are V_o=5.00V. For computing the efficiency, the theoretical value (0.6434) is also very close to the simulated value (0.6436). To maximize the efficiency, we may re-compute δ to obtain δ_{opt}=0.2134, and the corresponding η_{max} is 0.6449. From (95), the coefficient of $(\Delta\delta/\delta_{opt})^2$ is 0.652, with $\Delta\delta$ = 0.2134–0.192 = 0.0214, and $\Delta\delta/\delta_{opt}$=0.1. The efficiency is then η = 0.6449 – 0.652×0.1^2 = 0.6384. Two conclusions can be drawn: (i) the estimated η using (95) is less than 1% from the computed value; and (ii) even with a 10% deviation from δ_{opt}, the resultant efficiency is still very close to η_{max}. A plot of η versus δ in the vicinity of δ_{opt}, along with Cadence simulations, is shown in Fig. 15.

Table 5. Comparison of analyses with simulations.

	Analysis	**Simulation**	**% error**
[5] with N=5, C=5pF			
V_o	5.000V	4.960V	0.8%
η	66.67%	64.47%	3.41%
[6] with N=5, C=5pF			
V_o	4.9604V	4.960V	0.008%
η	65.19%	64.47%	1.12%
This work with N=5, C=5.21pF			
V_o	5.00V	5.00V	0%
η	64.34%	64.36%	0.031%
This work with N=5, C=4.72pF			
V_o	4.894V	4.902V	0.020%
η	64.49%	64.51%	0.031%

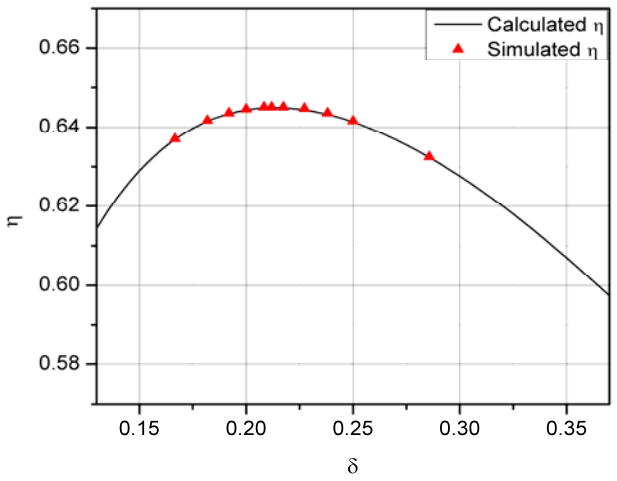

Fig. 15. Simulated η vs δ in the vicinity of δ_{opt} with α=0.01.

11 Conclusions

In this research, charge balance law is systematically employed to analyze charge pumps with ideal switches and finite positive-plate and negative-plate parasitic capacitors. Equations for output voltages, output voltage ripples and efficiencies are derived for single-branch and dual-branch linear charge pumps. In computing $V_o(t)$, a finite load capacitor C_L is used, and the result is extended to $C_L=\infty$. We observe that C_L determines the output voltage ripple, but has a negligible effect on the average output voltage. From exact derivations, it is found that V_{o2} is independent of C_L for both single-branch and dual-branch charge pumps, and can be used to simplify analysis for $C_L=\infty$. Interpolation could then be performed to obtain V_{o1} and V_{o3} for single-branch charge pumps, and V_{o1} for dual-branch charge pumps.

Besides linear charge pumps, Fibonacci and exponential charge pumps are analyzed. The exact analysis of FQPs and EQPs are too complex and no insight could be obtained. Instead, we proposed a first iteration approximation analysis to obtain reasonably accurate results. Our findings are as follows. (1) If $C_L=\infty$, the performance of single-branch and dual-branch charge pumps are the same, and the single-branch LQP is preferred due to its lower complexity. (2) If parasitic capacitors are negligible, LQP, FQP and EQP give the same total capacitance for the same output voltage. (3) In the presence of parasitic capacitors, LQP is the best topology that could achieve the highest output voltage.

Efficiency optimization of LQPs is through first computing the optimal number of stages, followed by finding the reduction factor δ that achieves the required average output voltage V_o. Using δ_{opt} to maximize the efficiency η may not be necessary as the sensitivity of η w.r.t. δ is very low. From the obtained δ we may then choose to

change either the flying capacitor C or the switching frequency f_s or both for the design. All the analyses are confirmed by Cadence Spectre simulations.

11 References

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