# Self-Timed Rings: A promising Solution for Generating High-Speed High-Resolution Low-Phase Noise Clocks

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**Abstract.** A high-speed multi-phase oscillator based on self-timed ring is proposed. Self-timed rings (STR) are promising approach for designing high-speed serial links and clock generators. Indeed, the architecture of STR allows us to achieve high frequencies with multiphase outputs and their oscillation frequency is not only depending on the number of stages but also on the initial state of the ring. Moreover, this architecture allows us 3 dB phase noise reduction when, while keeping the same frequency, when the stage number is doubled. In this chapter, we propose a method to design STR able to generate high-speed multi-phase outputs and we suggest a design flow for designing low-phase noise self-timed ring oscillators. A test chip has been designed and fabricated in STMicroelectonics CMOS65nm technology to verify the theoretical claims and validate the simulation results.

**Keywords: ring oscillators, self–timed rings, asynchronous logic, low-phase noise, multi-phase oscillators.**

## 1 Introduction

Oscillators are essential building blocks in many applications. They are basic blocks in almost all designs: they are part of PLLs, clock recovery systems and frequency synthesizers. The design of low phase-noise multi-phase clock circuitry is crucial especially when a large number of phases is required. There are plenty of works covering the design of multiphase clocks [2-4] [18-21]. High frequency oscillators can be implemented using ring structures, relaxation circuits or LC circuits. Ring architectures can easily provide multiple clocks with a small die size.

Multiphase clock generation have two important features: the frequency and the resolution. We mean by resolution the lowest time interval between two phases of the multiphase oscillator output. High frequencies with a high resolution are often required in multiphase clocks. The inverter ring oscillators are usually used to produce such a clock generator. The main problem we face with inverter rings for implementing multiphase clocks is the exponential frequency drop with respect to the number of phases. In inverter ring oscillators, the frequency is only determined by the number of stages and the stage delay. Moreover, their resolution is limited to the stage

delay and the only way to obtain more output phases is to add more stages, which decrease the maximum frequency and do not improve the resolution. Consequently, inverter-ring oscillators cannot be used in applications requiring high resolution or high-speed multiphase clocks.

For example, an important application that cannot use ring oscillators is precision waveform timing generation for single-chip testers [1]. When testing digital integrated circuits, the delay resolution which is required to have accurate measurements is often smaller than the gate delay of the device under test. This fine resolution can only be obtained with ring oscillators by using a higher speed integrated circuit technology for the tester than for the device under test. The main problem with inverter rings is the frequency drop when a large number of phases is required. It exists many architectural techniques which have been proposed to increase the maximum frequency of ring oscillators with multiphase outputs. Some of these techniques include the use of sub-feedback loops, output-interpolation methods [2], skewed delay schemes [3], multiple-feedback loops [4] and coupled oscillators [5]. However, these techniques require careful calibration to achieve high precision, their resolution is limited and the extra hardware increases the phase noise.

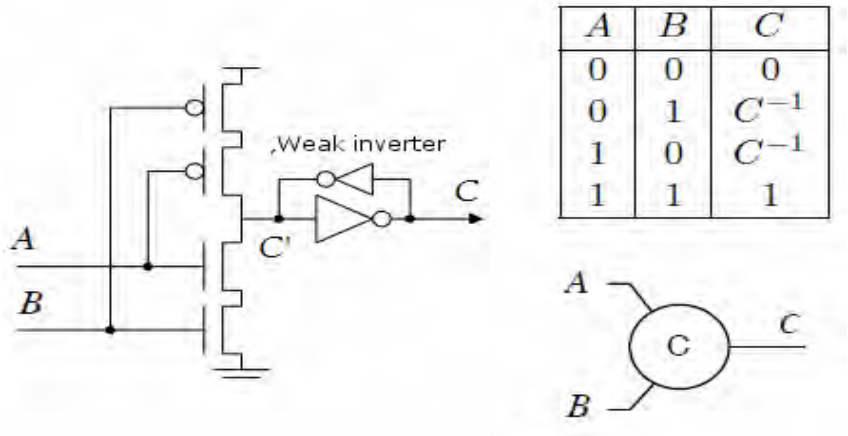
With the advanced nanometric technologies, it is required to deal with the process variability, the stability and the phase noise. Today many studies are oriented to Self-Timed Ring (STR) oscillators which present well-suited characteristics for managing process variability and offering an appropriate structure to limit the phase noise. Therefore self-timed rings are considered as promising solution for generating clocks. S. Fairbanks and S. Moore in [6] introduced the idea of the use of self-timed rings to generate high-resolution timing signals. Their robustness against process variability in comparison to inverter rings is proven in [7]. Moreover, self-timed rings can easily be configured to change their frequency by just controlling their initialization at reset time. At the opposite, inverter rings are not programmable. A Fully programmable/stoppable oscillator based on self-timed rings is also presented in [8].

This paper proposes a methodology to generate high-speed multi-phase clocks based on Self-timed rings. The oscillation frequency in STR does not only depend on the number of stages, but also on the initialization. We explain how this configurability can be used to reduce the phase noise by simply doubling the number of stages without changing the oscillation frequency. The article is structured as follows. Section 2 provides the background, definitions and principles of Self-timed Rings. Section 3 present the different CMOS implementations of Muller's C-element with is the main component of the self-timed rings. Section 4 explains the design rules to have high-speed multiphase oscillators. Section 5 shows how to reduce by -3dB the phase noise in STR by simply doubling the stage number while maintaining approximately the same frequency and the same resolution. Section 6 shows how this kind of oscillators can be used to generate à quadrature output signals. In section 7, we show how we can extend the frequency range thanks to the configurability. Section 8 proposes a design flow for implementing low-phase noise multiphase oscillators. Finally, Section 9 states the conclusions and future works.

## 2. Self-Timed Rings

### 2.1 Architecture

The C-element is the basic element in asynchronous circuit design, introduced by D. E. Muller. C-elements set their output to the input values if their inputs are equal and hold their output otherwise. Figure 1 shows a possible CMOS implementation where the initialization circuit is omitted. C-element implementations are detailed in section 3.




| A | B | C |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | $C^{-1}$ |
| 1 | 0 | $C^{-1}$ |
| 1 | 1 | 1 |

**Fig. 1.** Muller's C-element

Each stage of STR is composed of a C-element and an inverter connected to the input B. The input which is connected to the previous stage is marked F (Forward) and the input which is connected to the following stage is marked R (Reverse), C denotes the output of the stage, as shown in Figure 2.

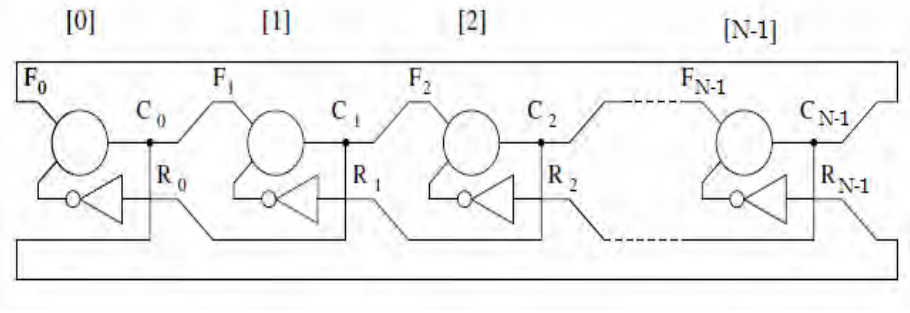



**Fig. 2.** A self-timed ring

### 2.2 Tokens and bubbles

This subsection introduces the notions of Tokens "T" and Bubbles "B" which are very important to understand the behavior of the STR. $Stage_i$ contains a token if its output $C_i$ is not equal to the output $C_{i+1}$ of $stage_{i+1}$. On the other hand, $Stage_i$ contains a bubble if its output $C_i$ is equal to the output $C_{i+1}$ of $stage_{i+1}$.

$$C_i = C_{i+1} \Rightarrow Stage_i = \{Bubble\}$$
$$C_i \neq C_{i+1} \Rightarrow Stage_i = \{Token\}$$

The number of tokens and bubbles will be respectively denoted $N_T$ and $N_B$. For keeping the ring oscillating, $N_T$ must be an even number; this can be interpreted as an analogy when designing an inverter ring with a odd number of stages. Each stage of the STR contains either a token or a bubble. Notice that $N_T + N_B = N$, where N is the number of the ring stages.

### 2.3 Propagation rules.

If a token is present in $stage_i$, it will propagate to $stage_{i+1}$, if and only if $stage_{i+1}$ contains a bubble. The Bubble of $stage_{i+1}$ will move backward to $stage_i$. This implies a transition on $stage_{i+1}$ output. For example, hereafter the token/bubble movements in a five stage STR which contains 4 token and one bubble. The stage outputs are given between the parentheses.

Example: TTBTT (01001)➔ TBTTT (01101)➔ BTTTT (00101)➔ TTTTB (10101)➔ TTTBT (10100) ➔ TTBTT (01001)

Self-timed rings produce two different modes of oscillation: "Evenly spaced" or "Burst" modes. In the evenly spaced mode, the events inside the ring are equally spaced in time. In the burst mode, the events are non-uniformly spaced in time. In our application, we only target the evenly spaced mode.

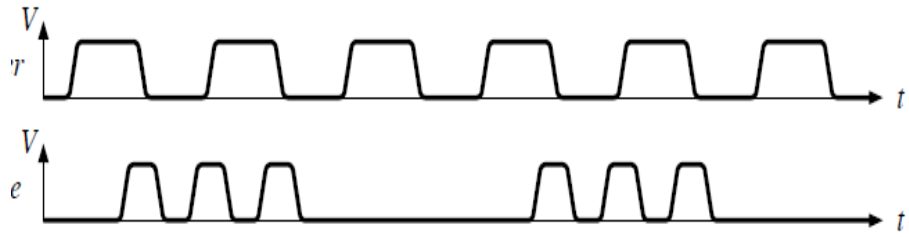



**Fig. 3.** Modes of Operation in Self-Timed Rings (Evenly spaced and burst mode)

### 2.4 Configurability

The oscillation frequency in STR depends on the initialization (number of tokens and bubbles). The oscillation frequency in a self-timed ring can be approximated according to the number of tokens and bubbles by the following formula [9]:

$$F_{OSC-STR} = \frac{1}{2.D.(R+1)} \quad (1)$$

$$(D,R) = \begin{cases} (D_{rr}, N_T/N_B) & \text{if} \quad D_{ff}/D_{rr} \le N_T/N_B \\ (D_{ff}, N_B/N_T) & \text{if} \quad D_{ff}/D_{rr} \ge N_T/N_B \end{cases}$$

where $D_{ff}$ is the static forward propagation delay from input F to the output C and $D_{rr}$ is the static reverse propagation delay from input R to the output C. The maximum frequency is achieved when $D_{ff}/D_{rr}=N_T/N_B$. This equality also ensures the evenly spaced propagation mode [7].The output number in STR is equal to the number of stages. The number of the different phases is determined by the number of stages in which the Token/Bubble combination allows us to have an irreducible ratio $N_T/N_B$. For instance, if we double the number of stages in the 5-stage example (4T and 1B; $N_T/N_B=4/1$), the ring will have ten phases (8T and 2B; $N_T/N_B=8/2=4/1$). However, only five of them are different phases. Each phase of the five "new" phase signals will be in phase with one of the five "original" phase signals. The resolution can be calculated by $T_{ph}=T/N_{min}$. Where T is the oscillation period and $N_{min}$ is the number of minimum stages to have an irreducible ratio $N_T/N_B$ (which is 5 in the above example).

### 2.5 Modified Stage

In the STR architecture depicted in Figure 2, we have $D_{ff} > D_{rr}$. Therefore to achieve the maximum frequency with multiphase outputs, a higher number of bubbles than the number of tokens is required.

In order to have more flexibility in design and to improve the performance of the self-timed ring, we propose a modified ring stage. The modified stage is simply a C-element, without the R input inverter. We just interconnect the ring structure thank to the complementary outputs C' (which is natively available in a C-element structure but rarely used). Note that the complementary output is obtained from the internal structure of the C-Element (Figure 1) without any additional hardware. For each stage the output C is connected to the following stage input F and the complementary output C' is connected to the previous stage input R (Figure 4).

This modified self-timed ring (MSTR) stage allows us to improve the maximal speed by 30%. With such a modified structure, we can achieve a maximal frequency of 8.3 GHz in CMOS 65 nm. This modified structure of STR, in addition to the standard STR, offers more design flexibility to achieve high frequencies with a large number of multiphase outputs.

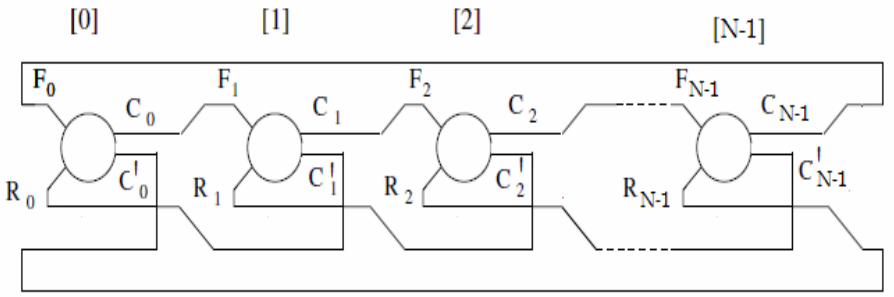



**Fig. 4.** Modified Self-Timed Rings

## 3. C-element implementations

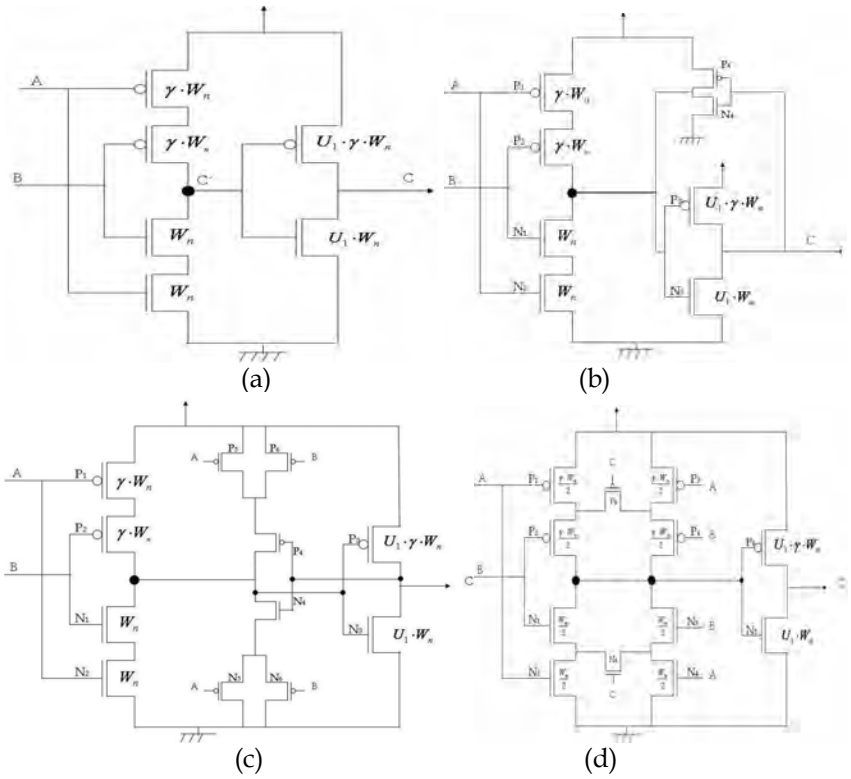



**Fig. 5.** C-element implementations: Dynamic (a), weak feedback (b), conventional(c) and Symmetric (d)

This section presents different implementations of the C-element. In addition to the dynamic implementation [17], there are different static implementations of the C-element in the literature such as the Weak-feedback by Martin [14], the Conventional by Sutherland [15] and Symmetric by Van Berkel [16].

The dynamic implementation [13] (Figure 5.a) is composed by an output inverter and the main stack of transistors of the C-element. These transistors called “switchers” contribute to the switching of the output.

For the static implementations, in addition to the “switchers” we have a mechanism for memorizing the output value; these transistors are called "keepers". The "keepers" are not active during the switching, they just provide a feedback to maintain the output state when the input values are different, so they are as small as possible to reduce their load and limit their current [17]

The weak feedback implementation of the C-element is shown in Figure 5.b; this implementation is composed by the same “switchers” of the dynamic one, in addition to a weak-reaction inverter (N4 and P4) to maintain the state of the output. This circuit suffers from a race problem at node C’.

In the conventional implementation (see Figure. 5.c), in addition to the weak-feedback inverter, we have four additional transistors (N5, N6, P5 and P6) to disconnect this weak-feedback inverter when the inputs are equal. N4, N5, N6, P4, P5 and P6 are sized at the minimal width allowed by the technology.

The C-element introduced by Van Berkel is illustrated in Figure 5.d. This implementation is slightly different from the previous ones. The transistors are split in two parts. The "keepers" are N4 and P4 and the splited transistors are also involved in the state holding.

## 4. Designing high-speed Multiphase oscillators

In inverter-ring oscillators, the oscillation frequency and the number of phases depends on the number of inverters.

$$F_{OSC-INV} = \frac{1}{2.D_{inv}.N} \tag{2}$$

where $D_{inv}$ is the inverter delay and N is number of stages. The number of different equidistant phases is equal to the number of stages N. Oscillation frequency is inversely related to the number of stages and the number of phases is directly related to the number of stages. This implies an inverse relation between the number of phases and the oscillation frequency. The more multiphase outputs the more the frequency drops. Some solutions have been proposed to increase speed but this improvement is really limited in the case of a large multiphase output number [2] [3] [4].

In STR oscillators, the oscillation frequency does not depend on the number of stages but depends on the ratio $N_T/N_B$. To achieve a high frequency with multiphase outputs, we have to choose $N_T/N_B$ as near as possible to $D_{ff}/D_{rr}$ with the condition that $N_T/N_B$ is irreducible. The oscillation frequency is related to the ratio $N_T/N_B$ (not the

number of stages) and the number of phases is related to the number of stages (with the condition $N_T/N_B$ irreducible). This implies no direct relation between the number of phases and the oscillation frequency. This enables STR to increase/decrease their number of phases while maintaining a same oscillation frequency.

Table 1 presents the oscillation frequency and the number of equidistance phases produced for several rings based on modified stages with $D_{rr}$=21.3ps and $D_{ff}$=38.2ps (measurements in CMOS 65 nm technology from STMicroelectronics). We choose $N_T/N_B$ as near as possible to $D_{ff}/D_{rr}$. This table shows that we achieve a high frequency and multiphase outputs at the same time. With larger rings, we have more possibilities to find $N_T/N_B$ near to $D_{ff}/D_{rr}$ which achieves the maximum frequency allowed by the ring. For example, 41-stage ring achieve an oscillation frequency of 7.19 GHz with 41 equidistant phase outputs and a 3.4 ps resolution.

**Table 1.** Frequency and number of phases for several configurations (Drr=21.3ps and Dff=38.2ps)

| **N** | **$N_T$** | **$N_B$** | **$N_{Ph}$** | **Frequency (GHz)** |
|---|---|---|---|---|
| 3 | 2 | 1 | 3 | 4.32 |
| 4 | 2 | 2 | 4 | 6.31 |
| 5 | 2 | 3 | 5 | 4.64 |
| 6 | 2 | 4 | 6 | 7.02 |
| 7 | 4 | 3 | 7 | 6.95 |
| 8 | 6 | 2 | 8 | 5.75 |
| 9 | 4 | 5 | 9 | 5.69 |
| 10 | 6 | 4 | 10 | 7.10 |
| 11 | 6 | 5 | 11 | 5.81 |
| 13 | 6 | 7 | 13 | 5.89 |
| 14 | 6 | 8 | 14 | 5.50 |
| 15 | 8 | 7 | 15 | 6.71 |
| 16 | 10 | 6 | 16 | 7.18 |
| 17 | 10 | 7 | 17 | 7.05 |
| 18 | 10 | 8 | 18 | 6.83 |
| 19 | 12 | 7 | 19 | 7.18 |
| 31 | 18 | 13 | 31 | 7.01 |
| 41 | 24 | 17 | 41 | 7.19 |

Figure 6 displays the oscillation frequency with respect to the number of phases produced by a conventional STR, a modified STR, a conventional inverter ring, Sun's[2] and Lee's solutions[3]. Note that the results of [2] and [3] have not been simulated but estimated according to the percentage improvement reported in the papers [2] and [3] compared to the conventional inverter ring. Only the conventional STR, the modified STR and the inverter ring have been implemented and simulated. In the work of Sun et al. [2], the topology is based on the use of interpolated inverter stage outputs for constructing fast sub-feedback loops in a long chain. The gain in speed with this topology is about 70% compared with conventional inverter ring. Lee's technique [3] uses inverters with negative delays; the speed was improved by 50% compared to a classical inverter ring.

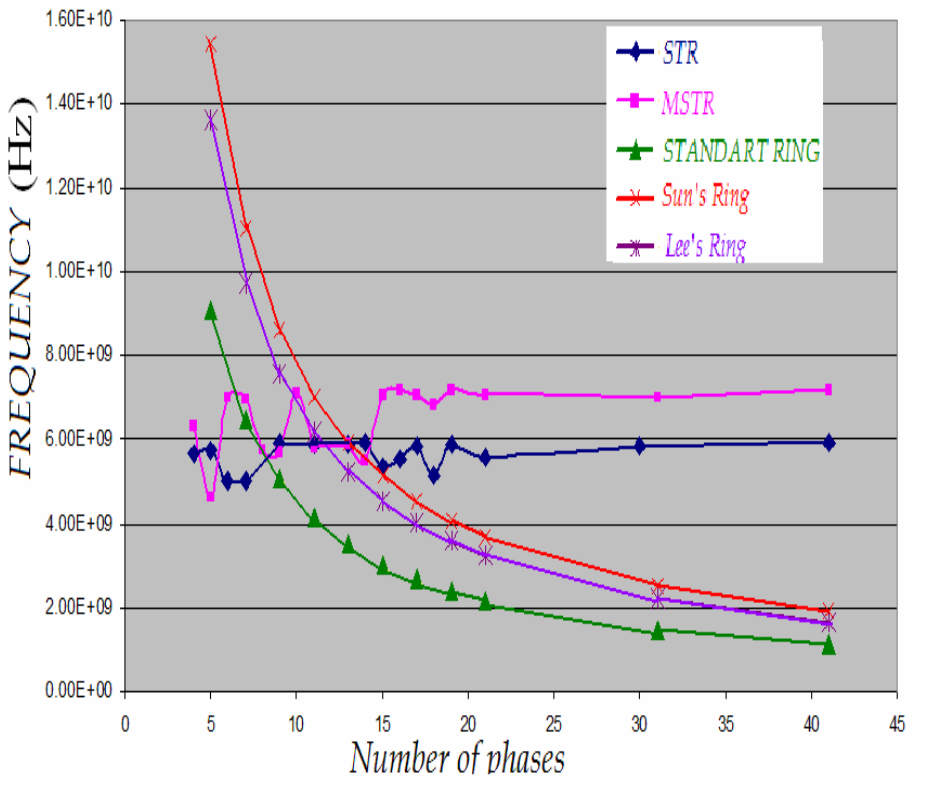



**Fig. 6.** Comparison between Inverter-Ring and STRs

As shown in the Figure 6, inverter rings can achieve higher frequencies when low numbers of phases are required. However, when a large number of phases is targeted, inverter rings loose their advantage. This comparison shows that using STR to generate high speed evenly-spaced multiphase clocks is the best choice if a large number of phases is required. Indeed, the frequency depends on the STR initial state

and increasing the number of stages does not necessarily means decreasing the speed. The resolution of the STR is one of the most promising advantages because they are able to increase their phase number while keeping approximately the same oscillation frequency. This leads to a resolution enhancement for these multiphase oscillators. For instance, using 31 stages (as in Table 1) produces an output frequency of 7 GHz, 31 phases and a resolution of 4.6 ps. With 41 stages, we achieved slightly higher frequency with 41 evenly-spaced phases. Moreover, the resolution of the 41-stage STR is better (3.4 ps). This result is clearly not achievable with inverter rings; their resolution always remains determined by their stage delay.

Table 2 presents the performances of the three multi-phases oscillators. We designed these three oscillators by respecting the rules given in section III. The temporal parameters of the stages are $D_{ff}$=32.4ps d $D_{rr}$=42.4ps. To achieve the highest frequency with a maximum number of equidistant multiphase outputs (number of stages), we chose the Tokens/bubbles configuration with respect to $N_T/N_B \approx D_{ff}/D_{rr}$ and $N_T/N_B$ irreducible.

The 9-stage STR ring oscillates with a higher frequency than the two others because its $N_T/N_B$ ratio is the closest to $D_{ff}/D_{rr}$. This table shows that we can increase the resolution and reduce the phase noise by simply adding stages and maintaining the frequency. Compare to the 9-stage STR, the resolution of the 41-stage STR is improved by 4.5 times and the phase noise is reduced by 7.8dBc/Hz with a small change in the oscillation frequency. Notice that the oscillation frequency is totally independent of the ring size; the oscillation frequency of the 41-stage STR is higher than those of the 9-stage STR. Figure 7 shows the multiphase outputs generated by the 41 stage STR.

**Table 2.** Several Self-Timed Rings with $N_T/N_B \approx D_{ff}/D_{rr}$

| Nb of stages | T/B | Frequ. (GHz) | Comsu. (mW) | Nb of phases | Resolution (ps) | PN at 1 MHz |
|---|---|---|---|---|---|---|
| 9 | 4/5 | 6.41 | 1.94 | 9 | 17.3 | -82.9 |
| 21 | 10/11 | 6.16 | 4.47 | 21 | 7.7 | -87.6 |
| 41 | 20/21 | 6.02 | 8.62 | 41 | 4 | -90.7 |

Table 2 shows that in addition to the improved resolution, the increase of the stage number also improves the phase noise. We improved the phase noise by 7.8dBc/Hz when we increase from 9 to 41 the stage number. At first glance this may appear absurd. How can we improve the phase noise by adding extra hardware? The explanations are given in the following section.

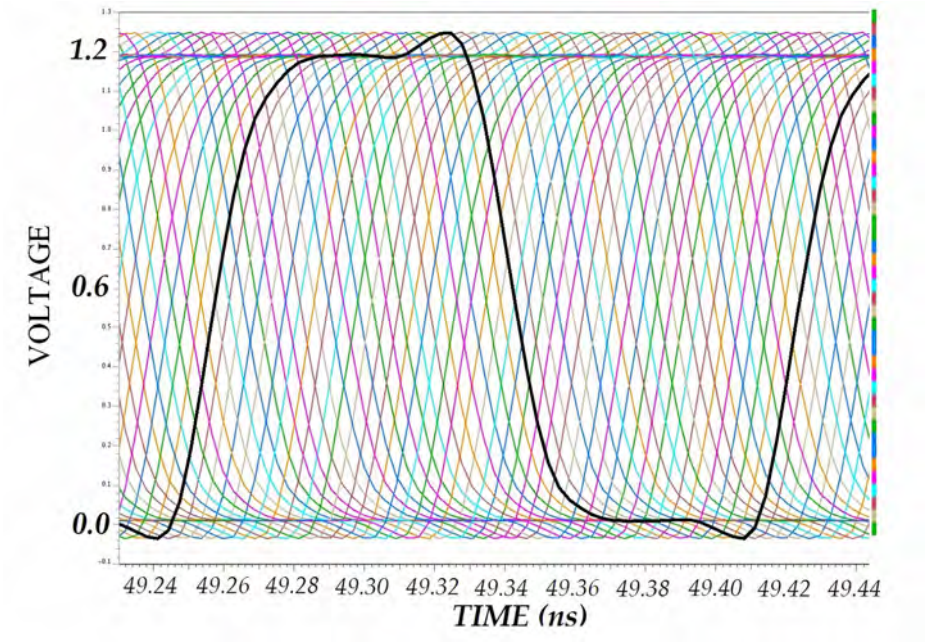



**Fig. 7.** 41 multiphase outputs generated by STR at 6.02 GHz.

## 5. Phase noise analysis

The noise in the MOS transistors is usually splitted into two contributions: the thermal noise and the flicker noise. The thermal noise is responsible of the noise floor at high frequencies while the flicker noise is reflected by a noise rise at low frequencies. The up-conversion phenomenon of the amplitude noise into phase noise is complex and has different origins. However, beyond the offset frequency $f_0/2Q_{ch}$, HF thermal noise imposes a noise floor (see parameter definitions below).

The phase noise is given by the semi-empirical Leeson formula [11]

$$L(f_m) = 10 \times \log\left(\frac{1}{2}\left[1+\left(\frac{f_0}{2Q_{ch}f_m}\right)^2\left(1+\frac{f_c}{f_m}\right)\left(\frac{FkT_0}{P_s}\right)\right]\right) \quad (3)$$

where:

- $Q_{ch}$ : Loaded Q-factor.
- $f_0$ : carrier frequency.
- $f_m$ : Frequency offset.
- $f_c$ : Corner frequency.
- F : Noise factor.
- k : Boltzmann's constant,.
- $T_0$ : Temperature (290K).
- $P_s$ : Signal power.

The Figure Of Merit (FOM) is a parameter that allows oscillator comparison by standardizing the phase noise compared to the oscillation frequency and the power consumption. It is calculated using the following equation [12]:

$$FOM = L(f_m) - 20\log\left(\frac{f_0}{f_m}\right) + 10\log\left(\frac{P_s}{1mW}\right) \quad (4)$$

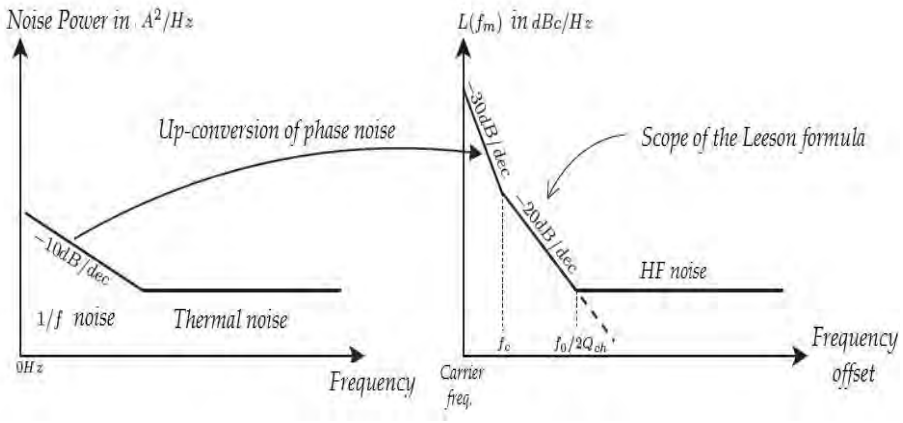



**Fig. 8.** Up-conversion of noise in oscillators

For two rings with different $\omega_n$ (NMOS width), which oscillate at the same frequency and consume the same amount of power, the ring with a larger $w_n$ will be better in term of phase noise. This is a result of the better characteristics of the falling and rising edges of the STR with larger $\omega_n$. This can be explained by the "Impulse Sensitivity Function" (ISF) introduced by Hajimiri [13] which represents the sensitivity to the signal disturbance. On one hand, when a pulse is injected during a transition, this results in a large phase shift. On the other hand, a pulse injection while the output is saturated has a minimal impact on the phase. Therefore the shorter the transition time, the less noise sensitive the signal.

Our experiments show that doubling the number of stages improves the phase noise by 3dB. According to Leeson's equation (3), there are two solutions to improve the phase noise: by improving the load factor Q or by increasing the signal power consumption Ps. The phase noise is inversely proportional to the oscillator power consumption. In other words, the phase noise can be reduced by 3dB by doubling the power consumption. The oscillators with the same ratio $N_T/N_B$ have the same waveform output signal and so have the same load factor.

According to B. Razavi [10], the load factor Q is expressed by:

$$Q = \frac{\omega_0}{2}\sqrt{\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\varphi}{d\omega}\right)^2} \quad (5)$$

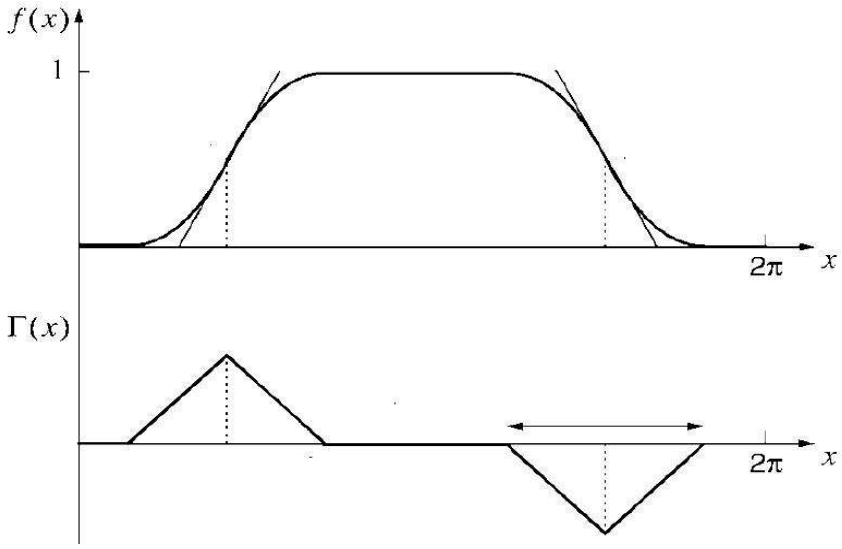



**Fig. 9.** Approximate waveform and ISF for ring oscillator

where A, φ and $\omega_0$ is the amplitude, phase and the signal pulsation.

In inverter ring oscillators, the only way to increase the signal power is to increase the transistor width $w_n$ and this implies a change in the oscillation frequency. On the contrary, we can increase the power consumption in STR while maintaining the same oscillation frequency; this is achievable by increasing the number of stages while maintaining the Token/Bubble ratio. This property is very attractive in STR oscillators because it allows us to have an additional degree of freedom during the design phase.

Another very important point is the symmetry between rising and falling edges; A.Hajimiri shows in [13] that the corner frequency $f_C$ is related to the symmetry between the edges.

$$f_C = f_{1/f} \cdot \frac{\Gamma_{dc}^2}{\Gamma_{rms}^2} \tag{6}$$

where $f_{1/f}$ is a 1/f noise corner frequency, $\Gamma_{dc}^2$ and $\Gamma_{rms}^2$ are the DC and the RMS values of the ISF.

We can see from the Figure 9 and equation (6) that the more symmetrical the edges, the closest to zero $f_c$. Therefore the symmetry between edges tends to reduce the phase noise.

Moreover, we can improve the resolution of the ring and reducing the phase noise in the same time by adding stages and choosing $N_T/N_B$ as near as possible to $D_{ff}/D_{rr}$ with the condition $N_T/N_B$ irreducible. With these rules, the maximal frequency remains the same, the resolution is improved and the phase noise is reduced. Table 3 presents the performances of STRs oscillators with the same Ratio $N_T/N_B$ =2. These oscillators are oscillating at the same frequency. The phase noise is reduced by -3db when the number of stages is doubled which confirms our analysis. Of course, it is not possible

to asymptotically create a zero phase noise ring having thousands of ring stages due to the noise floor imposed by the thermal noise (see Figure 8.).

**Table 3.** Self-Timed Rings with the same $N_T/N_B$ ratio

| N° of stages | T/B | Freq. (GHz) | Consum. (mW) | PN at 1M (dBc/Hz) | PN at 10M (dBc/Hz) |
|---|---|---|---|---|---|
| 3 | 2T/1B | 3.95 | 0.454 | -82.97 | -109.07 |
| 6 | 4T/2B | 3.95 | 0.908 | -85.98 | -112.08 |
| 9 | 6T/3B | 3.95 | 1.369 | -87.74 | -113.84 |
| 12 | 8T/4B | 3.95 | 1.817 | -88.99 | -115.09 |
| 15 | 10T/5B | 3.95 | 2.272 | -89.96 | -116.06 |
| 18 | 12T/6B | 3.95 | 2.726 | -90.75 | -116.85 |
| 24 | 16T/8B | 3.95 | 3.635 | -92 | -118.1 |

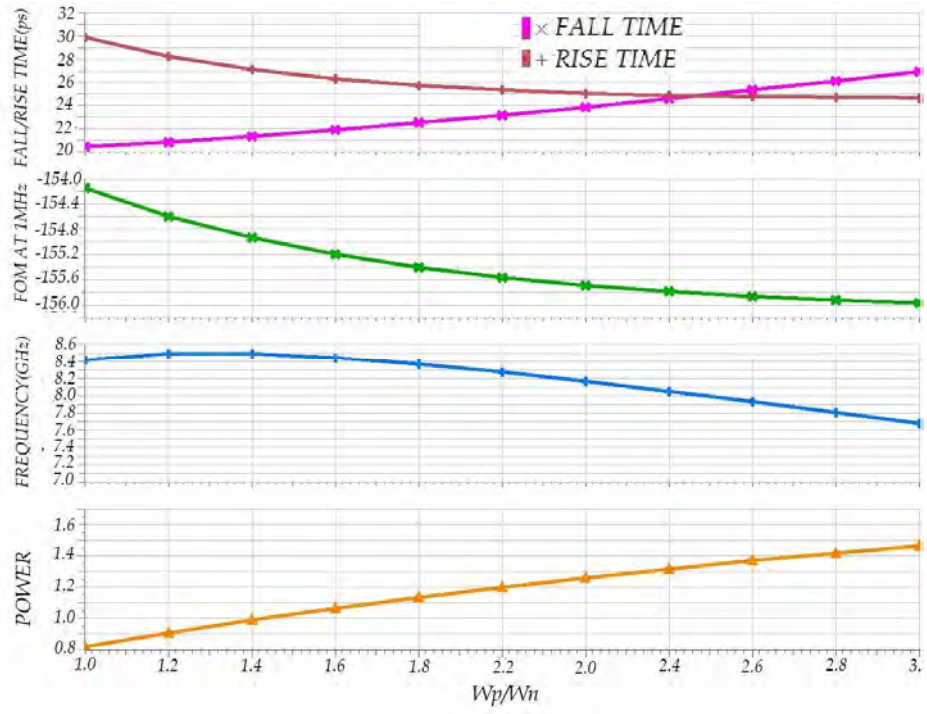



Fig. 10. FOM, frequency and power consumption vs. $\gamma = w_p / w_n$

Figure 10 shows the simulation results for a self-timed ring. The FOM, the frequency and the power consumption are plotted with respect to the $\gamma = w_p / w_n$ ratio ($w_n$ and $w_p$ are the NMOS and PMOS widths). We can see that the FOM is improved when the $\gamma$ ratio increased and reaches excellent values when the edges are almost symmetric ( $2 \le \gamma \le 3$ ). For high speed and low-power applications $1.2 \le \gamma \le 1.6$ would be a better compromise.

## 6. Quadrature signal generation

RF transmitter and receiver architectures use systematically frequency generators with quadrature output signals both in transmission and reception. The generation of signals in quadrature requires ring-based inverters with an even number of stages. However, it is unfortunately not possible with the standard structure of these oscillators. This requires the use of differential structures like CML "Current Mode Logic" [13] or feedback loops [2]. Many works deal with this subject [18-21].

Self-timed rings oscillators allow us to generate the quadrature output signals with a four stages oscillator initialized with two bubbles and two tokens. Indeed, it is the only configuration possible with this ring. We can also have quadrature output signals with multiple of four stages following the rules mentioned in section 3. Figure 11 shows the simulation results of a four stages self-timed ring. We notice a 90° phase shift between the four signals.

This oscillator has been designed using the conventional implementation of the C-element. The oscillation frequency is 5 GHz with a phase noise of -98dBc/Hz at 4 MHz offset and a consumption of 620µW. The phase noise is reduced 3dbc/Hz every time you double the number of stages. We get a figure of merit of -162dBc/Hz. Figure 12 shows the phase noise for this oscillator.

We conducted a comparison between the performance of this oscillator and the performances of published oscillators [18-21]. All these oscillators presented in the related articles are based on ring oscillators that generate quadrature phases designed in 0.18 microns technology in similar frequency ranges. Table 4 summarizes this comparison.

Table 4 shows that the self-timed ring oscillators are a serious alternative for the design of low-phase noise multiphase outputs oscillators. The FOM of our oscillator is -162dBc/Hz which is better than most of the cases presented in this table. The phase noise can be improved by duplicating the number of stages while remaining at the same value of the FOM.

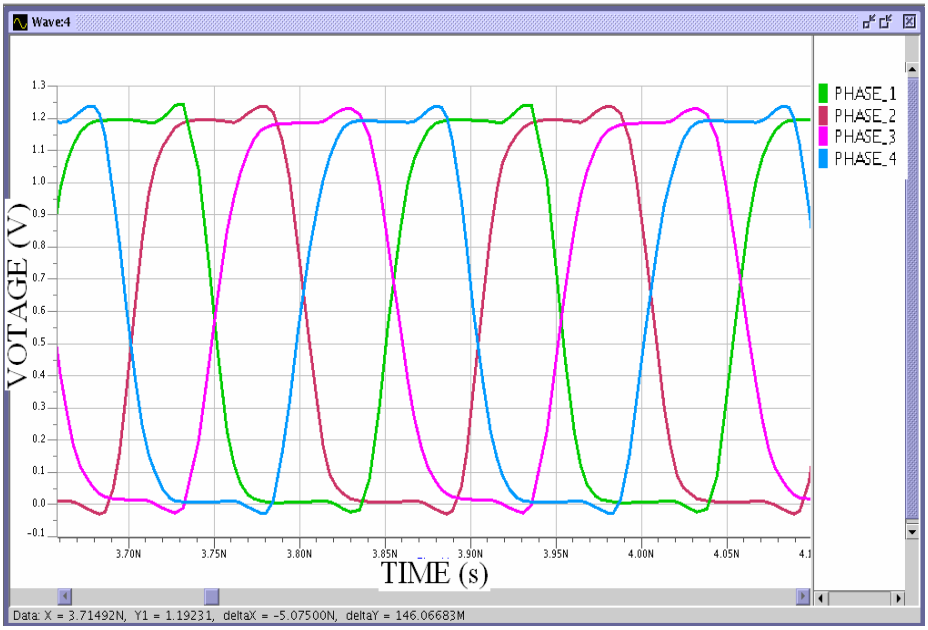



**Fig. 11.** Quadrature outputs of 2T/2B oscillator

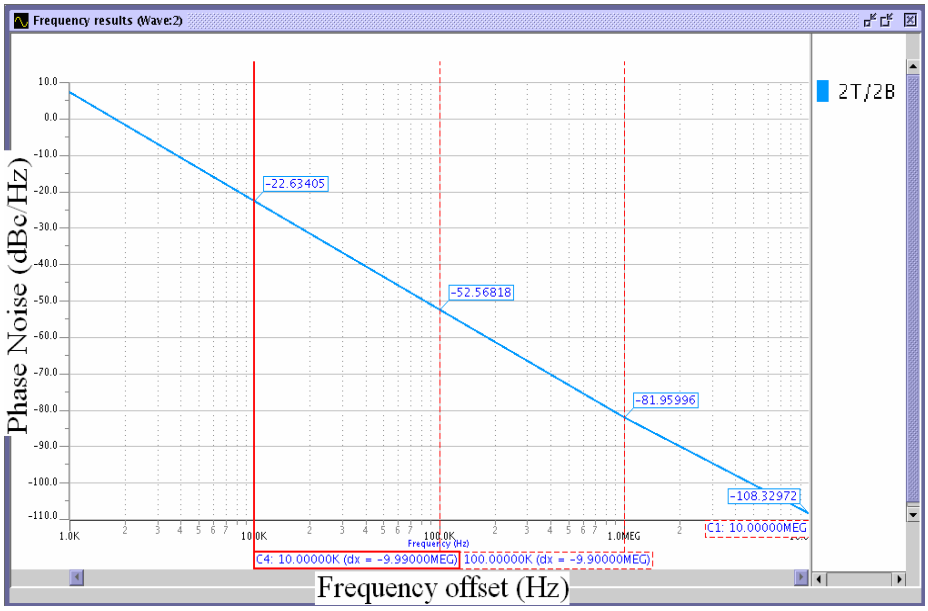



**Fig. 12.** Phase noise in 2T/2B self-timed ring oscillator.

**Table 4.** Comparison with previous works

| Ref. | Techno. | Freq. Max (GHz) | Conso. (mW) | Foff (MHz) | Phase noise (dBc/Hz) | FOM (dBc/Hz) |
|---|---|---|---|---|---|---|
| [18] | 0.18µm | 6.3 | 175 | 1 | -101.4 | -155.4 |
| [19] | 0.18µm | 3.5 | 16 | 4 | -106 | -152.7 |
| [20] | 0.18µm | 5.2 | 17 | 1 | -90.1 | -148.9 |
| [21] | 0.18µm | 5.5 | 81 | 4 | -116.06 | -162.2 |
| Our work (2T/2B) configuration | 65 nm | 5 | 0.62 | 4 | -98 | -162 |
| Our work (8T/8B) configuration | 65 nm | 5 | 2.5 | 4 | -104 | -162 |

## 7. Frequency range

Another important characteristic of self-timed rings, highly sought for the design of voltage controlled oscillator VCO, is the width of the frequency range [19]. Thanks to its configurability, we can design a VCO and coarsely tune its frequency by changing the tokens/bubbles configuration while the fine tuning is done with the classical voltage or current control techniques. For instance a 5-stage self-timed ring oscillator has two possible configurations: 2T/3B and 4T/1B. With 2T/3B configuration, the maximal frequency is reached. With 4T/1B configuration, the oscillation frequency is approximately divided by two. This oscillator produces five equidistant output signals with a 72° phase shift. We varied the supply voltage from 0.6V to 1.3V. The results are shown in Figure 13.

The frequency linearly varies with the supply voltage, which is preferable in voltage controlled oscillator (VCO) applications. In addition, the transition from one configuration to another one allows us to extend the frequency range.

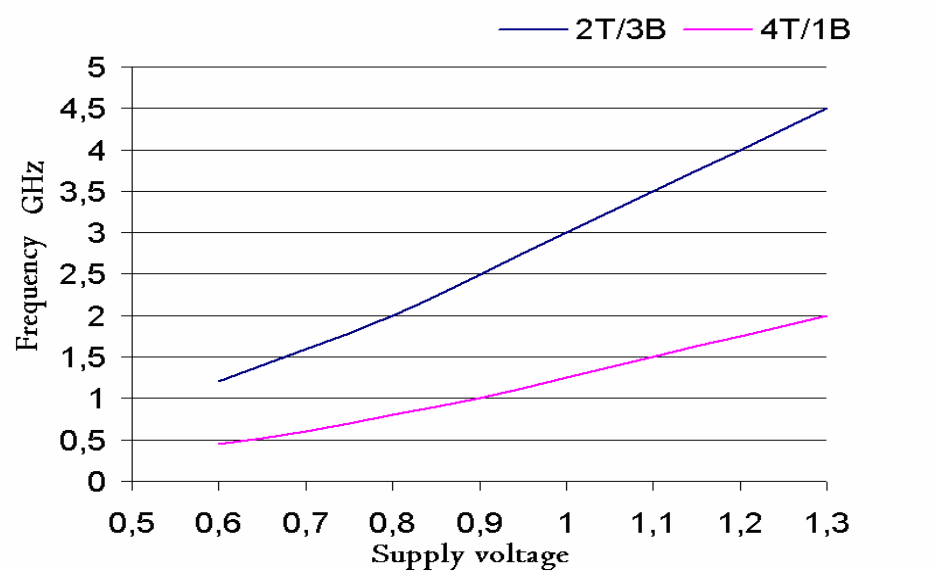



**Fig. 13.** Frequency Vs. Supply voltage.

## 8. A design flow for the self-timed ring oscillators

Figure 14 presents a design flow for the self-timed rings oscillators. According to the specifications, thanks to the frequency calculation equation (1) and according to $D_{ff}$ and $D_{rr}$, we can choose a preliminary architecture (number of stages, tokens and bubbles, stage implementation) which allows us to approach the targeted oscillation frequency and to reach the required number of phases. Moreover when we target multiphase oscillators, the tokens/bubbles ratio should be irreducible and as close as possible to the ratio $D_{ff}/D_{rr}$. In the case of quadrature outputs, a condition is added: the number of stages must be a multiple of four. $\omega_n$ can be adjusted to achieve the targeted frequency before starting the phase noise optimization. If the phase noise requirement is not satisfied, we have two choices:

- The first solution consists in reducing the phase noise of 3 dB by doubling the number of stages and keeping constant the ratio $N_T/N_B$. The great advantage of this approach is that the oscillation frequency remains unchanged.
- The second solution increases the $\omega_n$ of the transistors or optimizes the ratio $\omega_p/\omega_n$ in terms of FOM. This implies a modification of the frequency. In this case, the architecture is changed by another one with a different ratio R.

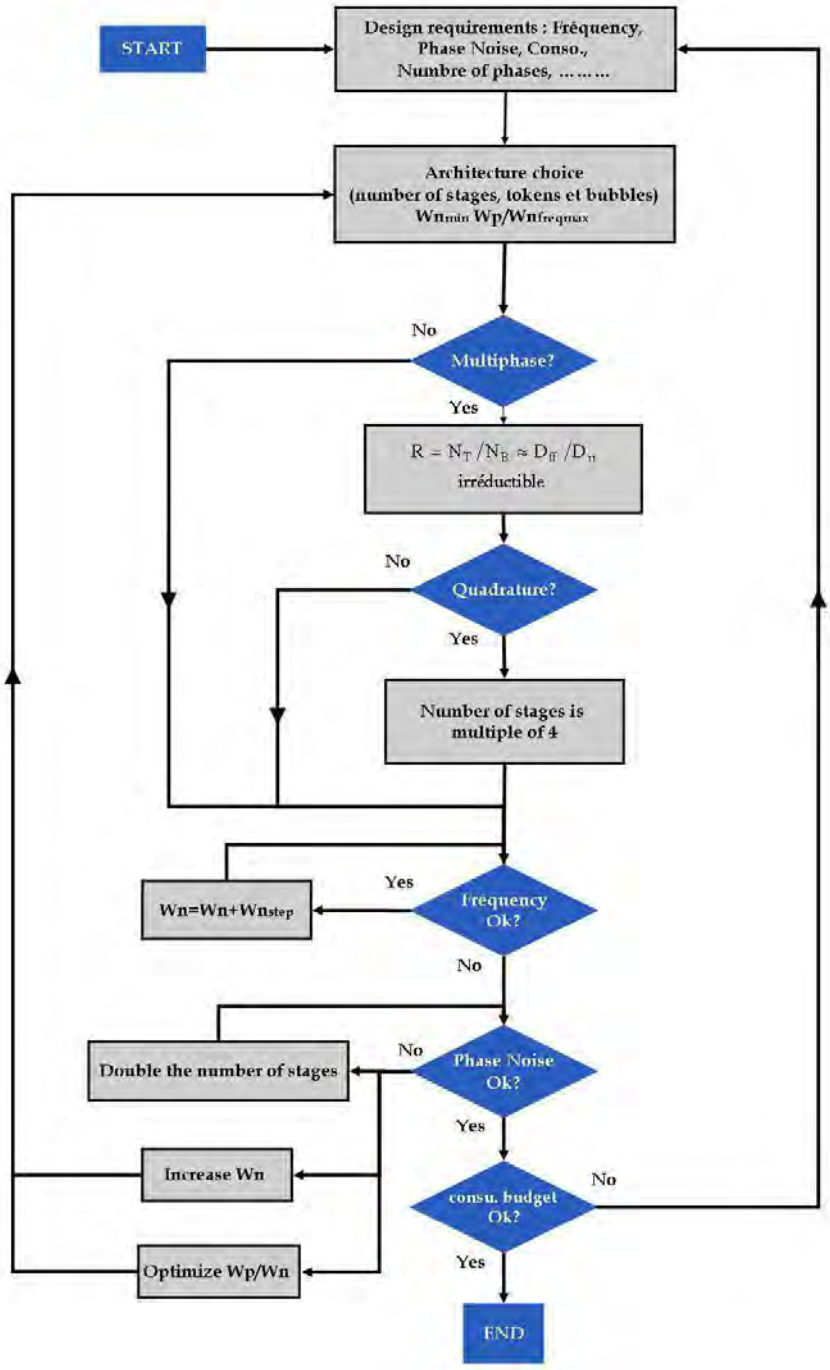



**Fig. 14.** Design flow for low phase noise Self-Timed Ring Oscillators

## 9. Conclusion

In this article, we presented a new oscillator topology based on self-timed rings for the generation of multiphase signals which are useful in many applications. Compared to inverter rings, one of the main advantages of the self-timed ring oscillators is their time resolution which is no more limited to the stage delay. Moreover, these oscillators are able oscillate at high frequency with a large number of multiphase outputs. A comparison with inverter ring oscillators clearly shows the advantages of our oscillators when a large number of phases is required. The self-timed ring oscillators are able to generate signals in phase quadrature which are especially useful in RF transmitters and receivers. A comparison with published studies shows the effectiveness of our method. In addition, we also demonstrated how to reduce the phase noise in self-timed rings oscillators by simply duplicating the number of stages. This feature provides to this type of oscillator an additional degree of freedom for designing s low-phase noise oscillator. In order to help the designers to implement such oscillators, a design flow dedicated to the self-timed ring oscillators is proposed. Finally, even if it is out the scope of this work which is focused on the self-timed ring design techniques, a test chip has been fabricated by STMicroelectronics in a CMOS 65 nm and the chip measurements confirm the relevance of our approach.

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