A CMOS Mixed-Mode Sample-and-Hold Circuit for Pipelined ADCs

Shan Jiang, Manh Anh Do, and Kiat Seng Yeo

Nanyang Technologies University,
School of Electrical & Electronic Engineering,
Block S1, 50 Nanyang Avenue,
Singapore 639798
shanjiang@pmail.ntu.edu.sg

Abstract. This paper describes the design of a high-speed CMOS sample-and-hold (S/H) circuit for pipelined analog-to-digital converters (ADCs). This S/H circuit consists of a switched-capacitor (SC) amplifier and a comparator to generate the mixed-mode sampled output data, which are represented both in analog and digital forms. The mixed-mode sampling technique reduces the operational amplifier (op amp) output swing. As a result, the requirements on op amp DC gain, slew rate and bandwidth are relaxed; the linearity of the SC amplifier is also improved. The reduction of signal swing in the front-end also brings benefit to the pipelined stages in speed and power consumption. The aperture errors at high frequency are minimized by time constant matching and digital error correction logic in the pipelined ADC. Designed in a 0.18-μm CMOS process, the proposed S/H circuit operates up to 200-MSample/s with a total harmonic distortion (THD) less than -60 dB and a signal-to-noise and distortion ratio (SNDR) larger than 59 dB in the worst-case simulation. The power consumption of the mixed-mode S/H circuit is 3.6-mW with 1.8-V supply voltage.

1 Introduction

The pipelined analog-to-digital converter (ADC) is one of the most popular converter architectures and has been widely used in many high-speed applications in wireless communication and video systems. Most pipelined ADCs include a sample-and-hold (S/H) circuit at the front-end to minimize the high frequency errors and to improve system performance. The performance of the S/H circuit dominates the overall ADC dynamic characteristics and plays a major role in determining the spurious free dynamic range (SFDR), signal-to-noise and distortion ratio (SNDR) of the system.

The stringent performance requirements of the S/H circuit make it the most design-challenging and power-hungry block in a pipelined ADC. Although a dedicated front-end S/H circuit can be removed and the sampling function is performed in the first stage of a pipelined ADC, the input capacitance of the pipelined ADC in this implementation is significantly increased due to the multi-bit first stage configuration [1]. A large input capacitance stresses the driving

circuit of the ADC, which usually is a variable gain amplifier (VGA). In some solutions, the full scale input range of the ADC is reduced and so is the achievable dynamic range [2]. The time constant matching is another concern in a pipelined ADC without a front-end S/H circuit. Although the aperture errors due to the time constant mismatch can be treated as comparator offset errors and removed by the digital error correction logic, due to the high gain of the multi-bit first stage, it is easy for the aperture errors to saturate the S/H circuit output swing. This sets a limit on the highest working frequency of the pipelined ADC without a front-end S/H circuit. Therefore, a dedicated front-end S/H is necessary in these considerations.

The performance of an S/H circuit is usually determined by an operational amplifier (op amp) in a switched-capacitor (SC) implementation. In an S/H circuit, the op amp must have enough DC gain to guarantee the accuracy requirement; and a fast slew rate and large bandwidth to meet the speed demand. The op amp performance also has an effect on the linearity of the S/H circuit, and consequently the overall ADC dynamic performance. Beyond these, in order to achieve a desirable signal-to-noise ratio (SNR), a large signal swing is required at the output of op amp even in the low voltage environment.

In high-speed low-power applications, it is always desirable to use the single-stage op amp architecture with the minimum transistor size whenever possible. This is due to the high-speed, low-noise, low-power and stability characteristics of the single-stage op amp. In practice, one of the challenges is that the DC gain of the single-stage op amp is limited unless larger transistors are use to increase the output impedance. However, a larger transistor size transfers into a lower speed because of the parasitic capacitance load. Another problem associated with single-stage op amp is the limited output signal swing due to the cascode operation, which leads to a limitation on the SNR and linearity. These challenges become more and more significant as the supply voltage and device size scale down.

This paper proposes a mixed-mode S/H circuit that reduces the requirements of op amp DC gain, slew rate, bandwidth, and output swing. The relaxation on performance requirements enables the use of single-stage cascode op amp in low voltage environment without degrading the system performance. The reduced requirements are accomplished through a built-in comparator in the S/H circuit. The aperture errors are minimized by time constant matching and digital error correction logic.

2 The Op Amp in the S/H Circuit

The schematic of a conventional fully differential switched-capacitor S/H circuit is shown in Fig. 1 [3]. In the sampling mode, switches S_1, S_2 and S_4 are on and S_3, S_5 off, the input signal is sample in C_S and the feedback capacitor C_F is reset. At the end of the sampling mode, S_2 turns off first, leaving the top plate of C_S floating to eliminate the signal-dependent charge-injection caused by S_1. Subsequently, S_1, S_4 turn off and S_3, S_5 turn on. The charges in C_S are

transferred to the feedback capacitor C_F. The output is given by

$$V_{out} = V_{in} \frac{C_S}{C_F + \frac{C_F + C_S + C_{in}}{A_0}} \tag{1}$$

where C_{in} is the input gate capacitance of op amp and A_0 is the op amp DC gain. If A_0 is large,

$$V_{out} \approx V_{in} \frac{C_S}{C_F} (1 - \frac{1}{\beta \cdot A_0}) \tag{2}$$

where $\beta = C_F/(C_F + C_S + C_{in})$ is the feedback factor in the holding mode. Equation (2) shows that there is a gain error of $1/(\beta \cdot A_0)$ due to the finite op amp DC gain.

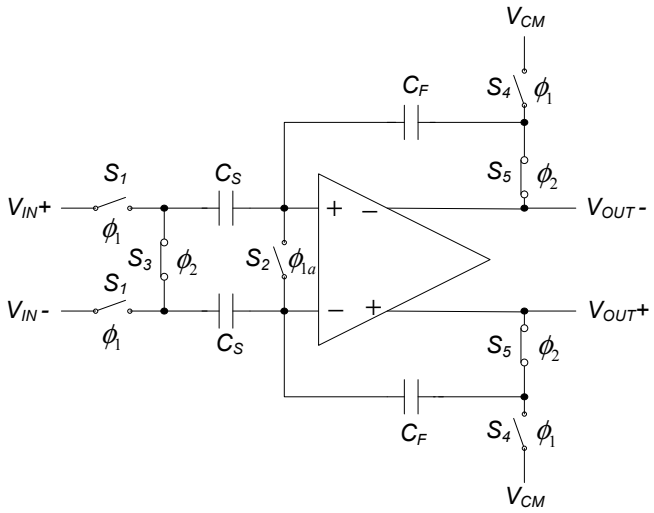

Fig. 1: SC implementation of a sample-and-hold circuit.

Assume this S/H circuit was used in an N-bit ADC, for a full scale step input, the output error due to finite op amp DC gain must be less than half of the least-significant-bit (LSB) in order to avoid introducing any error to the following pipeline stages This determines the minimum DC gain requirement of the op amp, which is

$$A_0 > \frac{1}{\beta} \times 2^{N+1} \tag{3}$$

Although an S/H gain error can be tolerated in some applications, the gain error drift must be minimized, which requires a high op amp DC gain across temperature and process corners.

2.1 Op Amp DC Gain Variation with Input Signals

The op amp DC gain depends on input and output signal swing, which can be illustrated by the differential amplifier shown in Fig. 2. In this amplifier, the current difference $\Delta I = I^+ - I^-$ can be expressed as [4]

$$\begin{aligned}\Delta I &= \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}V_{in}\sqrt{\frac{I}{\mu_n C_{ox}\frac{W_1}{L_1}} - V_{in}^2} \\ &= \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}V_{in}\sqrt{4(V_{GS}-V_{TH})_1^2 - V_{in}^2} \\ &= \mu_n C_{ox}\frac{W_1}{L_1}(V_{GS}-V_{TH})_1 V_{in} \times \sqrt{1 - \frac{V_{in}^2}{4(V_{GS}-V_{TH})_1^2}} \\ &= g_{m1}V_{in}\sqrt{1 - \frac{V_{in}^2}{4(V_{GS}-V_{TH})_1^2}} \end{aligned} \tag{4}$$

where L_1, W_1 and g_{m1} are the channel length, width and transconductance of M_1, respectively.

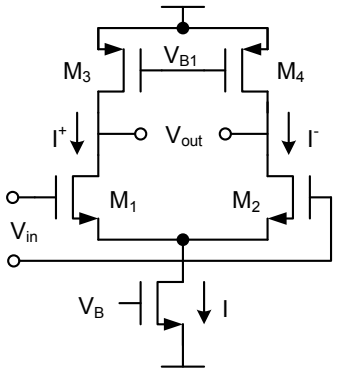

Fig. 2: A differential amplifier.

The output impedance of the amplifier is $r_{o1}||r_{o3}$. Assume $r_{o1} = r_{o3}$, the gain of the amplifier equals to

$$\begin{aligned} A &= \Delta I\frac{r_{o1}}{2}/V_{in} \\ &= g_m\frac{r_{o1}}{2}\sqrt{1 - \frac{V_{in}^2}{4(V_{GS}-V_{TH})_1^2}} \\ &\approx A_0(1 - \frac{V_{in}^2}{8V_{eff1}^2}) \end{aligned} \tag{5}$$

where $A_0 = g_{m1}r_{o1}/2$ is the amplifier DC gain when the output is zero. $V_{eff1} = (V_{GS} - V_{TH})_1$ is the input transistor overdrive voltage.

The discussion so far on the op amp DC gain dependence on input and output signals has been based on the assumption that the output impedance r_o of MOS transistor in the saturation region is constant during signal swing. This is approximately true for long channel device working at high voltage environment. In short channel device, however, r_o varies very much with the drain-to-source voltage V_{DS}. In saturation region, this dependence can be approximated as

$$r_o = \frac{2L}{1 - \frac{\Delta L}{L}} \frac{1}{I} \sqrt{\frac{qN_B}{2\epsilon_{si}}(V_{DS} - V_{dsat})} \tag{6}$$

The variation of r_o gives rise to nonlinearity in an op amp. The amount of nonlinearity is heavily depends on how much the output signal swing, i.e. how much the V_{DS} changes. In addition, the transistor transconductance g_m also varies with V_{DS}, which further exacerbates the op amp nonlinearity since the voltage gain is determined by $g_m \cdot r_{o1}$. This phenomenon becomes significant in cascode op amp as V_{DS} of the cascode devices change significantly during the operation. The g_m, r_o, and voltage gain of an op amp vary with the output is illustrated in Fig. 3, 4, and 5, respectively.

Because the voltage gain varies during the operation, the gain requirement in (3) should be the gain when a largest output swing is applied. At this condition, the required zero output op amp DC gain is usually much larger than (3).

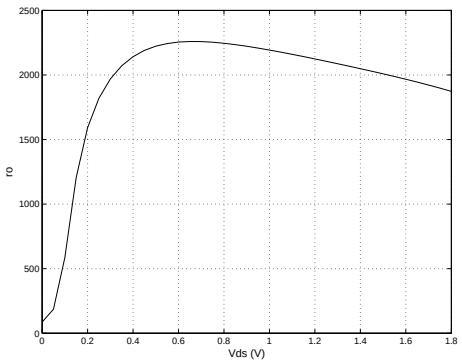

Fig. 3: g_m variation with output.

2.2 Nonlinearity Errors

The nonlinearity of the op amp DC gain is an important cause of nonlinearity errors in the S/H circuit. This harmonic distortion can be analyzed via charge

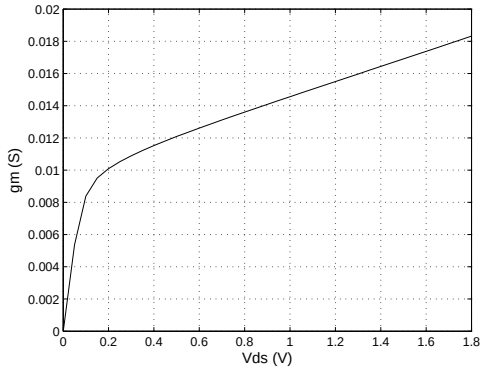

Fig. 4: r_o variation with output.

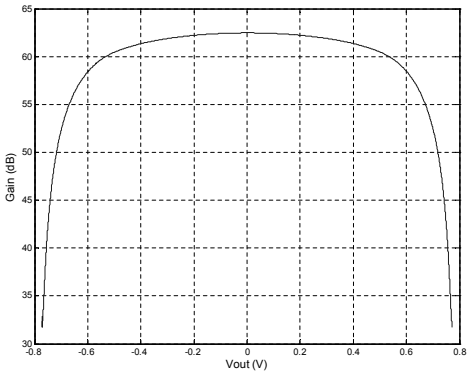

Fig. 5: A_0 variation with output.

conservation in a switched-capacitor circuit. If A_0 in (2) is replaced with A in (5), the transfer function of the S/H circuit in Fig. 1 can be written as

$$\begin{aligned} V_{out} &\approx V_{in}\frac{C_S}{C_F}(1-\frac{1}{\beta\cdot A}) \\ &\approx V_{in}\frac{C_S}{C_F}(1-\frac{1}{\beta\cdot A_0}\cdot\frac{1}{1-\frac{V'^2}{8V_{eff1}^2}}) \end{aligned} \tag{7}$$

V' is the voltage at the op amp input, which can be approximated as

$$V' \approx -\frac{V_{out}}{A_0} \approx -\frac{V_{in}\cdot\frac{C_S}{C_F}}{A_0} \tag{8}$$

Substitute (8) into (7), Vout can be expressed as

$$\begin{aligned} V_{out} &\approx V_{in}\frac{C_S}{C_F}[1-\frac{1}{\beta\cdot A_0}\cdot\frac{1}{1+\frac{V_{in}^2\cdot(C_S/C_F)^2}{A_0^2}}] \\ &\approx V_{in}\frac{C_S}{C_F}[1-\frac{1}{\beta\cdot A_0}\cdot(1-\frac{V_{in}^2\cdot(C_S/C_F)^2}{A_0^2})] \\ &= V_{in}\frac{C_S}{C_F}(1-\frac{1}{\beta\cdot A_0})+\frac{(C_S+C_F)^3}{\beta\cdot A_0^3}V_{in}^3 \end{aligned} \tag{9}$$

Equation (9) indicates the dependence of the S/H nonlinearity on the input signal. The above analysis doesn't take into account the nonlinearity due the device transconductance g_m and output impedance r_o variations with the output swing. This also contributes a large amount of nonlinearity but its derivation is tedious.

2.3 Op Amp Slew Rate and Bandwidth

The speed of an S/H circuit is determined by the settling time of the op amp in holding mode. The op amp settling time can be divided into two phases as shown in Fig. 6. The first phase is the nonlinear settling which is contributed by the slewing behavior of the op amp. The second phase is the quasi-linear settling which is contributed by the bandwidth of the op amp. For speed consideration, the slewing phase should be minimized, which requires a high op amp slew rate. The op amp with a high slew rate settles to the final value in the linear settling phase. Therefore even if the op amp is not fully settled at the end of the hold mode, there is only a linear error and an improvement of the dynamic performance can be expected. Since the slew rate of the op amp is determined by the output swing and the sampling frequency, a reduced output swing can improve the S/H accuracy and linearity.

In the linear settling phase, the op amp output settles exponentially towards its final value. If the op amp has one dominated pole and the second pole frequency is much higher, the output of the S/H circuit in Fig. 1 can be expressed as

$$V_{out}(t) = (1-e^{-\frac{t}{\tau}})V_{in}\frac{C_S}{C_F} \tag{10}$$

For the op amp incomplete settling introduced error to be less than LSB/2 of an N-bit ADD, the minimum value of op amp time constant τ should be

$$\tau < \frac{1}{2\cdot F_s\cdot(N+1)\cdot ln2} \tag{11}$$

where F_S is sampling frequency. The time constant τ can be further related to the op amp unity-gain bandwidth ω_u as

$$\tau = \frac{1}{\beta\cdot\omega_u} \tag{12}$$

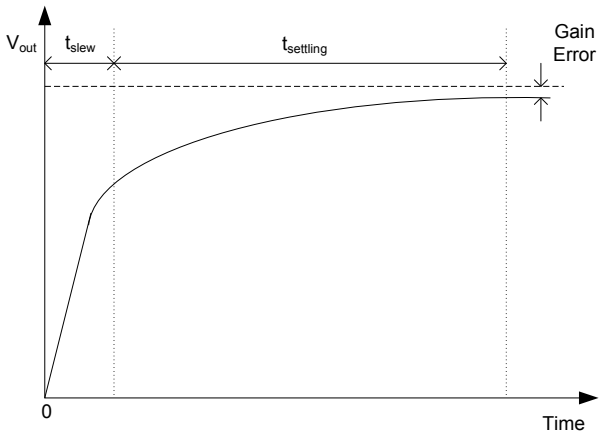

Fig. 6: Settling behavior of the op amp.

As a result, the op amp bandwidth requirement for an incomplete settling error smaller than LSB/2 is

$$\omega_u > \frac{2 \cdot (N+1) \cdot F_s \cdot ln2}{\beta} \tag{13}$$

3 The Mixed-Mode S/H Architecture

From above discussions, the variation of op amp DC gain with respect to the output swing introduces both gain error and nonlinearity in an S/H circuit. These errors become severe as the headroom left for the cascode device operation decreases in a low voltage environment. Although the single-stage op amp is preferred in high-speed applications, the error and nonlinearity often deprive its use ability in low voltage environment.

In order to exploit the single-stage op amp in low voltage environment, we propose a mixed-mode S/H circuit as shown in Fig. 7. One comparator is added to the conventional S/H circuit. The S/H operation is controlled by two non-overlapped clock phases, namely sampling phase ϕ_1 and holding phase ϕ_2. ϕ_{1a} is a copy of ϕ_1 but with an earlier falling edge. During the sampling phase, switches controlled by ϕ_1 and ϕ_{1a} are on, the sampling capacitor C_S is charge to $V_{in} - V_{os}$ with the aid of the virtual ground formed by the op amp in the unity-gain configuration. V_{os} is the offset voltage of op amp. Meanwhile, the feedback capacitor C_F is reset. The sampling phase ends at the falling edge of ϕ_{1a}. At the same clock edge, the comparator quantizes the input signal and generates the digital output D_{OUT}. Subsequently, ϕ_1 turns off the input switches and the bottom plate of C_S is connected to either $+V_{ref}/2$ or $-V_{ref}/2$, determined by the value of D_{OUT}. The S/H circuit is in the holding mode and the op amp offset is eliminated by the correlated double sampling [5]. As a result, for $C_S = C_F$,

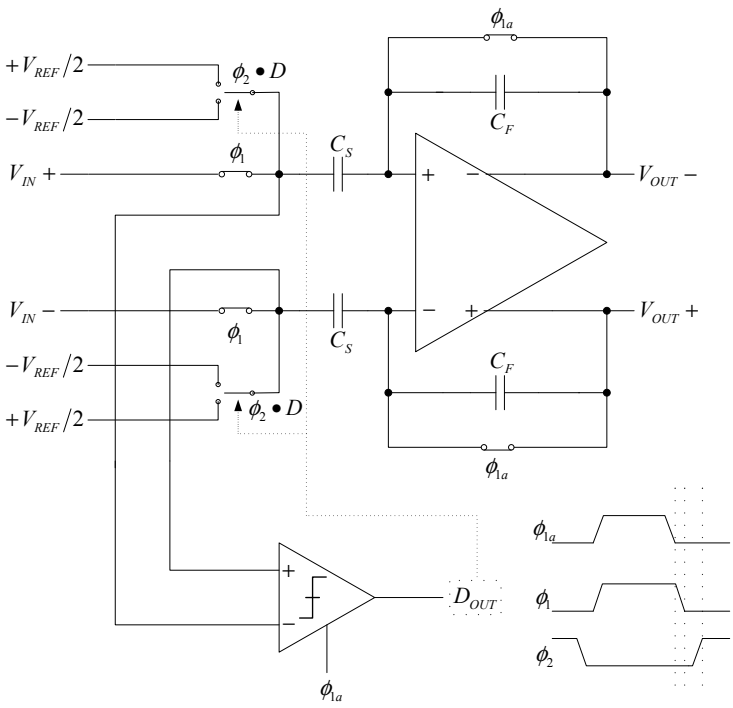

Fig. 7: The proposed mixed-mode sample-and-hold circuit.

the transfer function of the mixed-mode S/H circuit is given as

$$V_{out} \approx (1 - \frac{1}{\beta \cdot A_0})[V_{in} + (-1)^{D_{OUT}} \times V_{ref}/2] \tag{14}$$

where

$$D_{OUT} = \begin{cases} 1 \text{ for } V_{in} \geq 0 \\ 0 \text{ for } V_{in} < 0 \end{cases} \tag{15}$$

$$\beta = C_F/(C_F + C_S + C_{in}) \tag{16}$$

The sampled data is represented both in analog and digital forms. The transfer curve of this mixed-mode S/H circuit is illustrated in Fig. 8. Also shown is the one bit digital output send to the digital error correction logic. The dashed line shows the transfer curve of the conversional S/H circuit in Fig. 1 with C_S equals to C_F. As expected, the output swing of the proposed S/H circuit is the half of the full scale input range. The reduced analog signal swing doesn't degrade the SNR or stress the following pipelined stage since now the information is stored both in analog and digital forms and the full scale range is maintained.

Although the full scale input is unchanged, the effective input signal to the op amp is reduced by $V_{ref}/2$ as can be seen in (14). Therefore, the maximum

error introduced by finite op amp DC gain is $F_S/2\beta A_0$ in the proposed S/H circuit. If this S/H circuit is used in an N-bit ADC, for gain error to be less than LSB/2, we need

$$A > \frac{1}{\beta} \times 2^N \tag{17}$$

which is 6 dB lower than the requirement for the conventional S/H circuit as shown in (3). Although this configuration increases the error caused by finite op amp gain when the input is in the vicinity of zero as shown in Fig. 8, this error is still within the range of LSB/2 of the full scale. In addition, since the output swing is reduced, the DC gain is more stable, therefore an improvement of the S/H circuit linearity is expected.

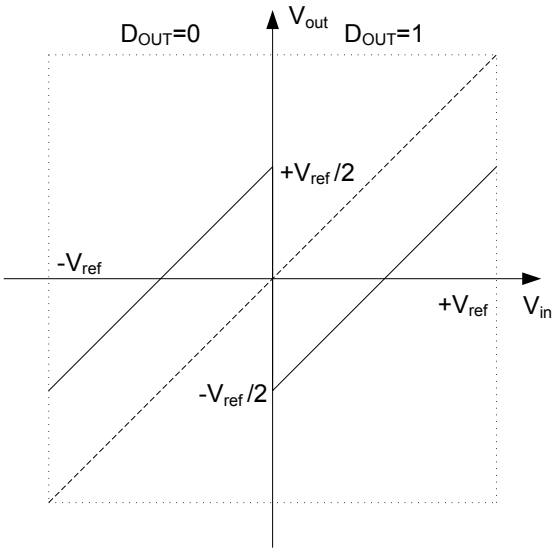

Fig. 8: The transfer curve of the proposed and conventional S/H circuit.

Since the output swing is halved, the required op amp unity-gain bandwidth in the mixed-mode S/H circuit becomes

$$\omega_u > \frac{2 \cdot N \cdot F_s \cdot ln2}{\beta} \tag{18}$$

which is smaller compare to the requirement of conventional S/H circuit expressed in (13).

The analog output of the mixed-mode S/H circuit will be processed by the following pipelined ADC stages. The 1-bit digital output will be combined with ADC outputs to generate the final output. Fig. 9 shows an example of the mixed-mode S/H circuit used in a 3-bit pipelined ADC. The S/H circuit has a 1-bit

output F_1. The final ADC digital output $D_2D_1D_0$ is the combination of the S/H output F_1 and pipeline stages' output $F_2F_3F_4F_5$.

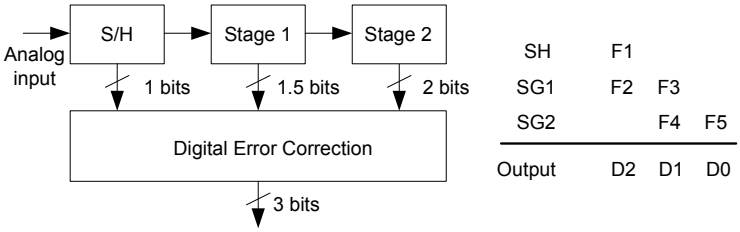

Fig. 9: The proposed S/H circuit used in a 3-bit pipelined ADC.

In a pipelined ADC, the op amp in the first pipeline stage has the most stringent requirements. Another benefit of the mixed-mode S/H is that since the output swing, which is the input of the first pipeline stage, is now reduced, the op amp gain and slew rate requirements in this stage are also relaxed based on the above observation.

Due to the additional comparator, in the sampling mode there are two signal paths in this S/H circuit. One is formed by the sampling switch, the sampling capacitor C_S and the op amp. The other goes through the comparator. Because of the time constant difference between these two paths, there exists a voltage error, i.e. the sampling capacitor C_S and the comparator see different input signals. The voltage difference is known as aperture error and will be increased with the input frequency. For an input signal of $V_{in} = V_{ref}sin(2\pi f_{in}t)$, the maximum slope of this signal can be presented as

$$\frac{dV_{in}}{dt} \mid_{max} = 2\pi f_{in} V_{ref} \tag{19}$$

Assuming the unmatched time constant between the two signal paths is $\Delta\tau$, the aperture error voltage, V_e, can be calculated as

$$V_e = 2\pi f_{in} V_{ref} \Delta\tau \tag{20}$$

Despite the existence of the aperture error, particularly at high frequency input, it is possible to minimize this error by matching the two signal paths in terms of topology and time constant. Fig. 10 shows the two signal paths during the sampling period. Instead of connecting the comparator directly to the input signal, it is connected to the output of the sampling switch. Thus the two paths see the same delay caused by the sampling switch. In addition, the op amp and comparator both use the falling edge of ϕ_{1a} to sample and quantize the input signal.

In actual implementation, it is difficult to match these two signal paths particularly at high frequency due to parasitic components and second-order effects.

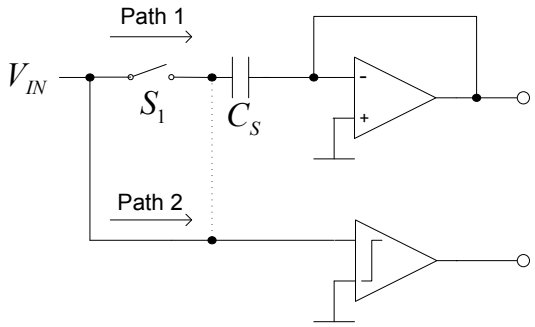

Fig. 10: The two signal paths in the sampling mode.

However, based on the characteristic of pipelined ADCs, the aperture error due to time constant mismatch can be treated as comparator offset error and eliminated by the digital error correction logic.

Although op amp and comparator offset errors can be tolerated in pipelined ADC by using digital error correction, these errors will increase the output swing, occupy a large offset correction range, and degrade the effective of the mixed-mode sampling technique. Therefore, in this design, auto-zero technique is used for the op amp in the sampling mode to eliminate its offset error. This is realized by connecting the op amp in the unity-gain configuration during the sampling mode. The comparator does not employ the auto-zero configuration because of the speed consideration. Otherwise the comparator has to quantize the input signal during the hold mode, which leads to a higher op amp speed requirement, or complicates the timing scheme that uses a shorter sampling phase to increase the time slot for amplifying.

4 Building Blocks

4.1 Operational Amplifier

Because the mixed-mode sampling technique reduces the signal swing and relaxes op amp gain and slew rate requirements, a gain-boosted single-stage telescopic op amp is use in the proposed S/H circuit as shown in Fig. 11. Transistors $M_1 \sim M_9$ forms the main telescopic op amp. Transistors $M_{B1} \sim M_{B7}$ provide the biasing voltages for the op amp. To improve the gain, transistors M_{10}, M_{12} and M_{11}, M_{13} form two common-source amplifiers and introduce negative feedback loops that make the source voltages of the common-gate transistors M_3 and M_4 less sensitive to the output signal. The gain boosting circuit increases the output impedance without adding more cascode devices. The gain boosting is only applied to the NMOS cascode transistors. The output impedance of the PMOS active load are increased by increasing the channel length of M_7 and M_8 since the size of these two devices have less effect on the op amp frequency

response. The overall DC gain of the gain-boosted telescopic op amp can be shown as

$$A_0 = g_{m1}\{[g_{m3}r_{o3}r_{o1}g_{m10}(r_{o10}||r_{o12})]||(g_{m5}r_{o5}r_{o7})\} \tag{21}$$

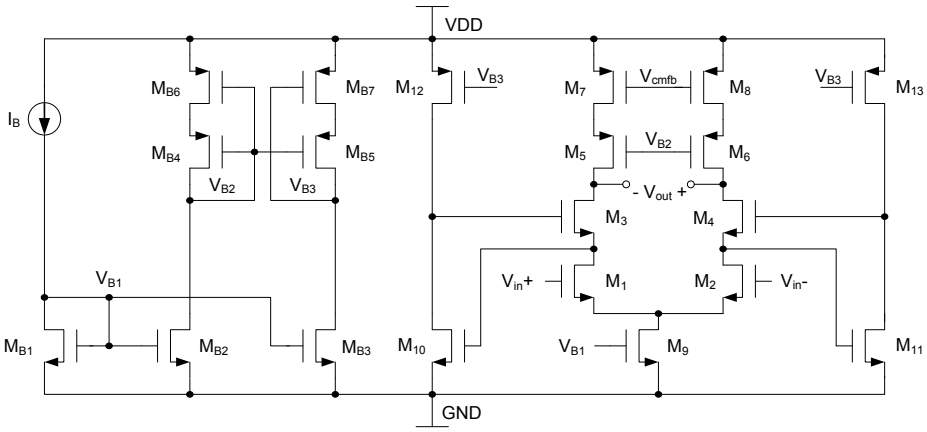

Fig. 11: The telescopic op amp with gain boosting.

It is clearly shown in (21) that the op amp DC gain depends on the transconductance of transistor M_1 M_3 M_5 and output impedance of M_1 M_3 M_5 M_7. In short channel devices, both g_m and r_o increase with V_{DS} before the devices reach drain-introduce barrier lowering (DIBL). In the mixed-mode S/H circuit, since the op amp output swing was reduced, the gate voltages of M_3 and M_5 are made high and low enough respectively to archive a higher DC gain. Fig. 12 shows the dependence of DC gain on output swing simulated with the slow MOS model. The simulation with the slow model gives the lowest available output swing which is the worst-case for accuracy and linearity. The simulated op amp has a DC gain of 64 dB, a phase margin of 70 degree and a unity-gain bandwidth of 1.1-GHz with 1-pF capacitive load as plotted in Fig. 13. The power consumption of the op amp is 2.8-mW at 1.8-V supply voltage.

For stability and settling considerations, the gain boosting circuit doesn't have to be very fast as long as its unity-gain frequency can satisfy

$$\beta\omega_{um} < \omega_{ug} < \omega_{np} \tag{22}$$

where β is the close-loop feedback factor, ω_{um} is the unity-gain bandwidth of the main amplifier, ω_{ug} is the unity-gain bandwidth of the gain-boosting amplifier and ω_{np} is the second-pole frequency of the main amplifier [6]. Special attention is paid to the position of the pole-zero doublet introduced by the gain-booting amplifier. Although this doublet does not deteriorate the op amp stability, it can affect the op amp close-loop settling time [7].

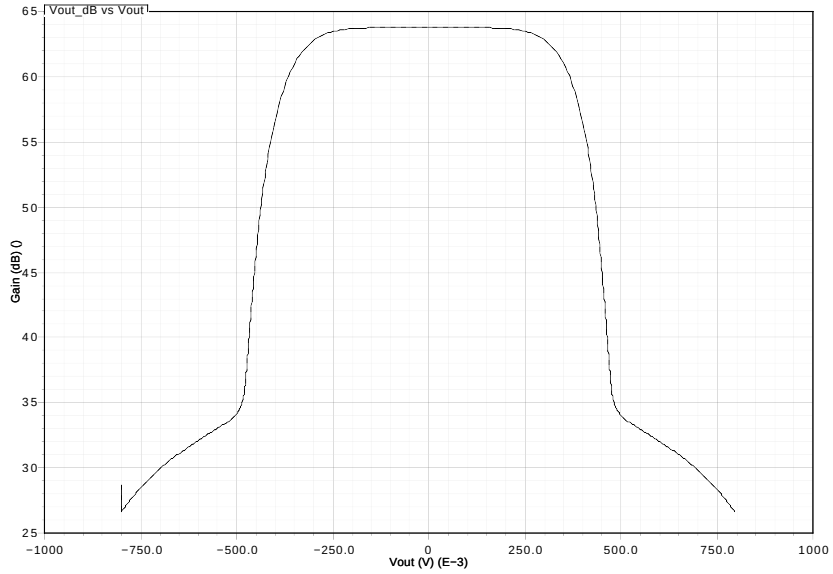

Fig. 12: Worst-case simulation of op amp gain variation.

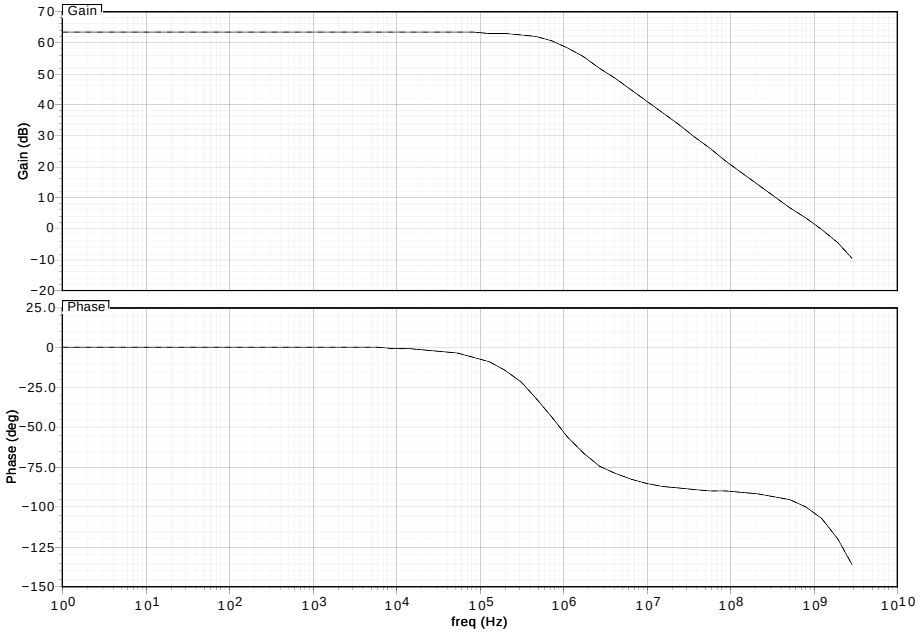

Fig. 13: The op amp gain and phase plot.

4.2 Comparator

The comparator used in the mixed-mode S/H circuit is shown in Fig. 14. The differential pair M_1 and M_2 amplify the input signal and transistors $M_4 \sim M_7$ form a regeneration latch. When ϕ_{1a} is high, $V_{out}+$ and $V_{out}-$ are reset to V_{DD} via M_8 and M_9. When ϕ_{1a} goes low, the differential pair M_1 and M_2 compare the input $V_{in}+$ and $V_{in}-$ and generate voltage difference at the drain of transistors M_4 and M_5. This voltage difference is amplified by the positive feedback of the latch therefore $V_{out}+$ and $V_{out}-$ goes to V_{DD} or ground according to the input voltages.

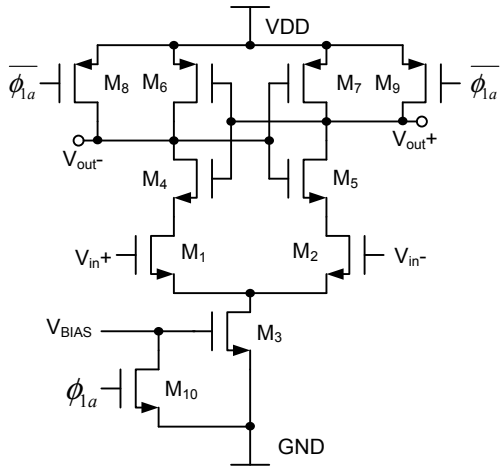

Fig. 14: The comparator used in the S/H circuit.

The offset of this comparator can be expressed as

$$V_{os} = \Delta V_{TH1,2} + \frac{(V_{GS} - V_{TH})_{1,2}}{2}\left(\frac{\Delta S_{1,2}}{S_{1,2}} + \frac{\Delta R}{R}\right) \tag{23}$$

$V_{TH1,2}$ is the threshold voltage mismatch of transistors M_1 and M_2. $\Delta S_{1,2}$ is the physical dimension mismatch between M_1 and M_2. ΔR is the load resistance mismatch, which is contributed by transistors $M_4 \sim M_7$. The offset voltage in this comparator is dominated by the mismatch between transistors M_1 and M_2. The mismatches caused by other transistors are reduced by the gain of M_1 and M_2. Besides increasing the size of M_1 and M_2, the offset can also be reduce by decrease $(V_{GS} - V_{TH})_{1,2}$, which is controlled by the tail current of the differential pair.

With manually introduced 20% device dimension mismatch, this comparator has an offset voltage less than 7-mV in worst-case simulation. This comparator achieves less than 300-pS regeneration time for a 1-mV differential input signal

in the worst-case simulation. The power consumption is 0.4-mW at 1.8-V supply voltage.

4.3 Bootstrapped MOS Switch

Besides the op amp, the input sampling switches also introduce nonlinearity due to its signal-dependent on-resistance. In order to investigate the error introduced by the op amp only. Bootstrapped MOS switches are used in the proposed S/H circuit. Fig. 15 illustrates the bootstrapped switch circuit [8].

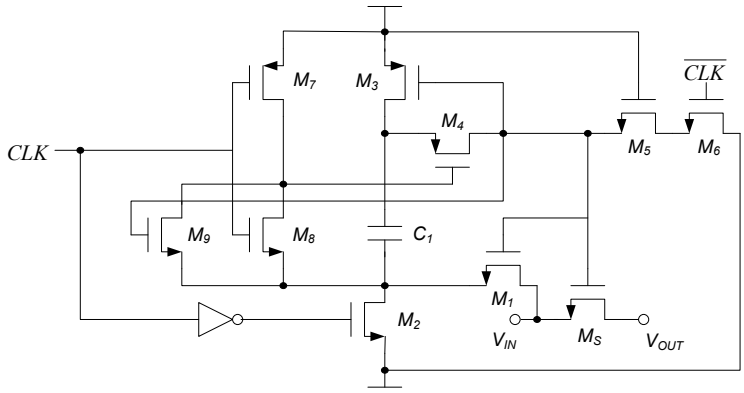

Fig. 15: The bootstrapped switch

The bootstrapped voltage is realized with the capacitor C_1, which is precharged to V_{DD} during the switch-off period. At the switch-on period, C_1 is connected between the gate and source terminals of the switch M_S via the switches M_1 and M_4. As a result, a constant gate-to-source voltage of V_{DD} applies to M_S, making its on-resistance independent of input signals.

5 Simulation Results

The proposed mixed-mode S/H circuit has been designed using a 0.18-μm CMOS process and simulated at worst-cast corner with manually introduced 7-mV comparator offset. The simulation is performed at 200-MHz sampling frequency and 1.8-V supply. Under these conditions, the S/H circuit consumes 3.6-mW.

Fig. 16 illustrates the digital and analog outputs of the mixed-mode S/H circuit at 200MSample/s with a 1-V_{PP} input sine-wave of 190-MHz (sub-sampling). It can be seen that the output swing is less than 540-mV with the aperture error and 7-mV comparator offset presented.

Plotting in Fig. 17 is the simulated SNDR, SFDR and THD as a function of the input signal frequency while the S/H samples at 200-MHz. The mixed-mode

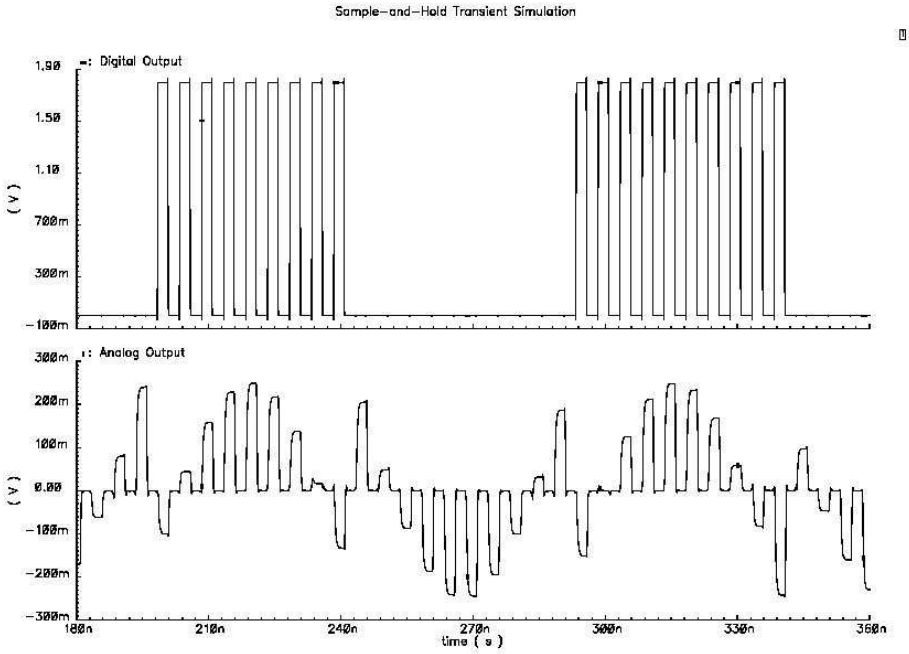

Fig. 16: Output waveform at 200-MSample/s with 190-MHz input.

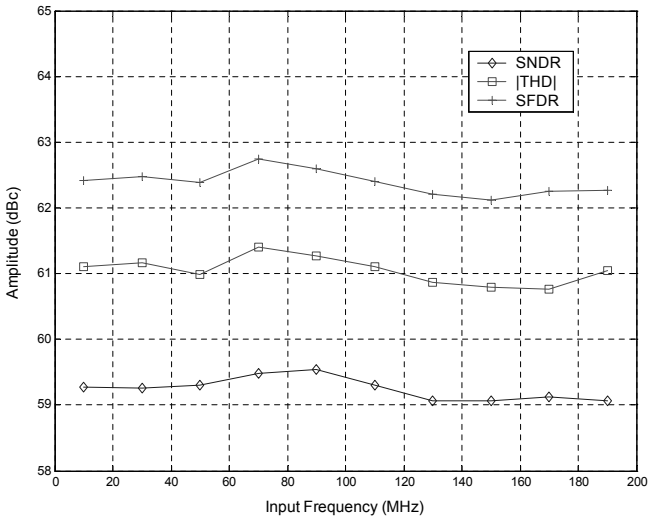

Fig. 17: Dynamic performance of the mixed-mode S/H circuits at 200-MSample/s.

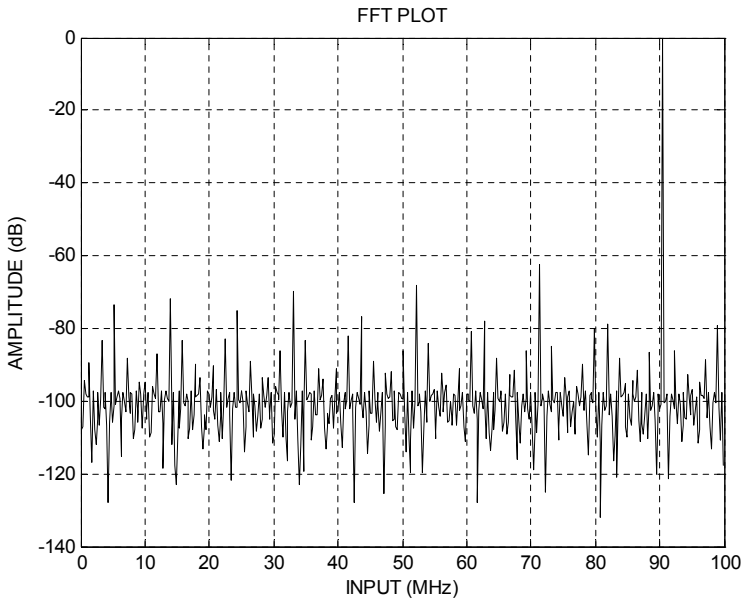

Fig. 18: Output spectrum with 200-MSample/s and 90-MHz input.

S/H circuit exhibits a THD lower than -60 dB and SNDR larger than 59 dB, i.e. better than 9-bit accuracy. The SNDR is larger than theory analysis in (17) because the linear settling behavior of the op amp. Fig. 18 shows the FFT plot of a 90-MHz input with 200-MSample/s, where about -61.2 dB THD and 59.5 dB SNDR are observed.

Table 1 summaries the simulated performance of the mixed-mode S/H circuit and compared it with the conventional S/H circuit in Fig. 1. Both the gain error and nonlinearity of the proposed mixed-mode S/H circuit are less than that of the conventional S/H circuit using the same op amp and switches.

Table 1: S/H circuit performance summary and comparison

Design	Mixed-Mode S/H	Conventional S/H
Technology	0.18-μm CMOS	0.18-μm CMOS
Power Supply	0.18-V	0.18-V
Sampling Frequency	200-MHz	200-MHz
SFDR	62.5 dB @ 90-MHz input	55.2 dB @ 90-MHz input
THD	-61.2 dB @ 90-MHz input	-53.2 dB @ 90-MHz input
SNDR	59.5 dB @ 90-MHz input	49.4 dB @ 90-MHz input
Power Consumption	3.6-mW	3.1-mW

6 Conclusion

In this paper, the design of a high-speed sample-and-hold circuit has been demonstrated by simulation results at 200-MSample/s. The proposed S/H circuits exhibits better linearity and lower power characteristic due to the mixed-mode sampling technique. This technique enables the use of single-stage cascode amplifier in the low voltage environment without degrading the dynamic performances and linearity.

References

1. D.-Y. Chang, "Design Techniques for a Pipelined ADC Without Using a Front-End Sample-and-Hold Amplifier," *IEEE Trans. Circuits and Systems I,* vol. 51, pp. 2123-2132, Nov. 2004.
2. H.-C. Kim, D.-K. Jeong, and W. Kim, "A Partially Switched-Opamp Technique for High-Speed Low-Power Pipelined Analog-to-Digital Converters," *IEEE Trans. Circuits and Systems I,* vol. 53, pp. 795-801, Apr. 2006.
3. I. Mehr and L. Singer, "A 55-mV, 10-bit, 40MSample/s Nyquist-Rate CMOS ADC," *IEEE J. Solid-State Circuits,* vol. 35, pp. 318-325, Mar. 2000.
4. B. Razavi,"Design of Analog CMOS Integrated Circuits," McGraw-Hill Higher Education, 2001.
5. C. C. Enz and G. C. Temes, "Circuit Techniques for Reducting the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," *Proceedings of the IEEE,* vol. 84, pp. 1584-1614, Nov. 1996.
6. K. Bult and G. J. G. M. Geelen, "A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain," *IEEE J. Solid-State Circuits,* vol. 25, pp. 1379-1384, Dec. 1990.
7. B. Y. Kamath, R. G. Meyer, and P. R. Gray, "Relationship Between Frequency Response and Settling Time of Operational Aplifiers," *IEEE J. Solid-State Circuits,* vol. sc-9, pp. 347-352, Dec. 1974.
8. M. Dessouky, A. Kaiser, "Input Switch Configuration for Rail-to-Rail Operation of Switched Opamp Circuits," *Electronics Letter,* vol 35, pp. 8-10, Jan. 1999.