Broadside Transition Test Generation for Partial Scan Circuits through Stuck-at Test Generation*

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Abstract. This paper presents a method of broadside transition test generation for partial scan circuits. The proposed method first transforms the kernel circuit of a given partial scan circuit into some combinational circuits. Then, by performing stuck-at test generation on the transformed circuits, broadside transition tests for the original circuit are obtained. This method allows us to use existing stuck-at test generation tools in order to generate broadside transition tests. It is shown that the proposed scheme is effective in area overhead and test generation time by experiments. In this paper, some variations of broadside transition testing of partial scan circuits are also discussed in terms of different test application strategies and fault sizes.

1 Introduction

Scan design is widely accepted by industry as an effective design for testability (DFT) method for delay faults as well as stuck-at faults. There is an essential difference between scan testing for stuck-at faults and that for delay faults. Unlike stuck-at testing, an additional consideration must be taken into account for delay testing using scan methodology. That is, to detect a delay fault, two consecutive vectors (two-pattern test) are needed to be applied to the faulty site in a scan environment. This can be done by using enhanced scan technique [7] or standard scan technique such as skewed-load technique [13] and broadside technique [14].

In [7], all the flip-flops (FFs) in a given circuit are replaced with enhanced scan FFs (ESFFs). Since each ESFF can store any two consecutive vectors, any two-pattern tests can be applied to the circuit. Although this method can drastically reduce the test generation complexity of a given circuit, its use is limited

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because of the considerable area and delay penalties incurred by ESFFs. For delay faults as well as stuck-at faults, full scan design is widely used as a DFT method. In delay testing, as mentioned before, two-pattern tests are required to detect delay faults, and they have to be applied by using scan FFs (SFFs), which can store any one vector. The skewed-load technique and broadside technique have been proposed as techniques to apply two-pattern tests to full scan circuits. In both of the techniques, the first vectors of two-pattern tests can freely be set to the SFFs through the scan chain. The second vectors are derived by shift operation in the skewed-load technique. In contrast, the broadside technique creates the second vectors by normal operation. In terms of feasibility, the broadside technique is more desirable than the skewed-load technique. This is because, in skewed-load testing, the scan signal is operated at the rated speed and it forces the scan chain to be designed judiciously. So far, there have been proposed several broadside test generation methods for full scan circuits [6, 17, 18, 20, 15, 2, 21].

Partial scan methodology is a viable solution to reduce the test generation effort of sequential circuits with reasonable area and delay overheads. For stuck-at faults, many researchers have considered partial scan design from various aspects. However, there are few works for delay faults in partial scan circuits. A transition test generation method, which is based on skewed-load testing, for partial scan circuits has been proposed in [5]. As mentioned previously, since skewed-load testing has some undesirable properties, a test generation method based on broadside testing is also needed for partial scan circuits. However, there have so far been no systematic approaches to generate broadside transition tests for partial scan circuits. In this paper, we tackle this problem. It is notable that broadside transition testing of partial scan circuits has a possibility of alleviating over-testing, which is one of the main concerns during testing [12, 1], in addition to reducing the penalties of area and delay.

In this paper, we propose a method to generate broadside transition tests for partial scan circuits. This method targets partial scan circuits whose kernel circuits are acyclic. To generate broadside transition tests for a partial scan circuit, we transform its kernel circuit into some combinational circuits. This transformed circuits are constructed by using a time-expansion model [8] of the kernel circuit. All the broadside transition tests are generated by performing constrained stuck-at test generation on the transformed circuits. Our method is effective in terms of ease of use because commercial stuck-at test generation tools, which are usually capable of handling combinational stuck-at test generation efficiently, can be used to generate broadside transition tests. By experiments, we show that our method can reduce area overhead and can generate broadside transition tests for partial scan circuits efficiently. In this paper, we also discuss some variations of broadside transition testing for partial scan circuits in terms of different test application strategies and fault sizes.

The rest of this paper is organized as follows. In Sect. 2, our target circuits and faults are explained, and previous work related to this paper is described. Section 3 presents a new test generation model to generate broadside transition

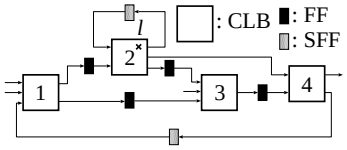

Fig. 1. Partial scan circuit: S

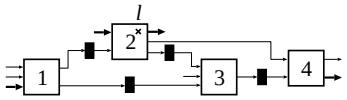

Fig. 2. Kernel circuit of Fig. 1: S_K

tests for partial scan circuits. Then, we give a test generation procedure using the new model, and the correctness of the procedure is proven. Experimental results are also presented in Sect. 3. We discuss some variations of broadside transition testing for partial scan circuits in Sect. 4. Section 5 concludes the paper and describes our future work.

2 Preliminaries

2.1 Target Circuits and Faults

In this paper, we handle partial scan circuits whose kernel circuits are acyclic. A sequential circuit can be represented as combinational logic blocks (CLBs) connected with each other directly or through FFs. A CLB is a region of connected combinational logic gates. An example of a partial scan circuit S and its kernel circuit S_K are shown in Figs. 1 and 2, respectively. The input (resp. output) of an SFF in Fig. 1 is treated as a primary output (PO) (resp. primary input (PI)) in Fig. 2, which is represented as a bold arrow and called a pseudo PO (PPO) (resp. pseudo PI (PPI)).

This paper tackles a broadside test generation problem for transition faults in a partial scan circuit. There are two transition faults associated with each line in a circuit: a slow-to-rise fault and a slow-to-fall fault. It is assumed that, under the transition fault model, the extra delay caused by a transition fault is large enough to prevent the transition through the faulty site from reaching any FF or any PO within a specified period. Note that, in a sequential circuit, different faulty behaviors can happen depending on the size of a transition fault [5, 21]. The size of a transition fault is defined as the amount of extra delay caused by the defect, and it is quantized by the number of clock cycles [5]. In this paper, although we concentrate on a transition fault whose size is one, the case where the size of a transition fault is more than one will be discussed in Sect. 4. This paper

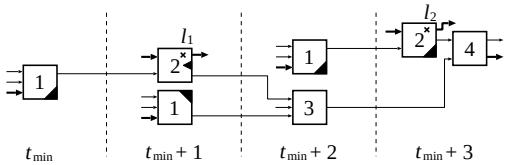

Fig. 3. Time-expansion model of Fig. 2: $C^T(S_K)$

assumes that transition faults in a partial scan circuit are tested in the slow-fast-slow testing manner [10] where a slow clock is used in the both of the fault initialization and fault effect propagation phases except in the fault activation phase. Under this assumption, we can consider a sequential circuit to be delay fault-free in both of the fault initialization and fault effect propagation phases. There are two possible strategies to apply a broadside transition test to a partial scan circuit. One strategy is called scan-per-vector [11] where scan operation is always allowed except in the fault activation phase. The other strategy is called scan-per-test [11] where scan operation is allowed only at the beginning of the fault initialization phase and at the end of the fault effect propagation phase. The former strategy is used in this paper. The discussion about the latter strategy will appear in Sect. 4.

2.2 Related Work

In this paper, we borrow an idea of a double time-expansion model, which is used to generate transition tests for an acyclic sequential circuit, from [9]. In [9], given an acyclic sequential circuit, a double time-expansion model of the circuit is constructed from a time-expansion model (TEM) [8] of the circuit. In the following paragraphs, we briefly explain those two models.

A TEM of an acyclic sequential circuit is a combinational circuit where the behavior of the original circuit within a specific time span is simulated. Figure 3 is a TEM $C^T(S_K)$ of the kernel circuit S_K shown in Fig. 2. TEM $C^T(S_K)$ is a combinational circuit derived by connecting CLBs according to their sequential depths. A sequential depth between two CLBs is defined as the number of FFs on a path between the CLBs. If a CLB has paths to another CLB in S_K whose sequential depths are different, the CLB is duplicated in $C^T(S_K)$. In Fig. 2, for example, since CLB 2 has two paths to CLB 4 whose sequential depths are different, CLB 2 is duplicated in $C^T(S_K)$. A shaded part of a CLB in Fig. 3 represents a portion of the lines and gates being removed. There is no path from the portion to any input of CLBs or any PO and PPO of $C^T(S_K)$. The character placed at the bottom of each frame in Fig. 3 is the label of CLBs in the frame, where $t_{\min}$ denotes an arbitrary integer. The label of a CLB v is denoted as $t(v)$ which corresponds to a specific time.

For an acyclic sequential circuit, its double time-expansion model is defined as follows [9].

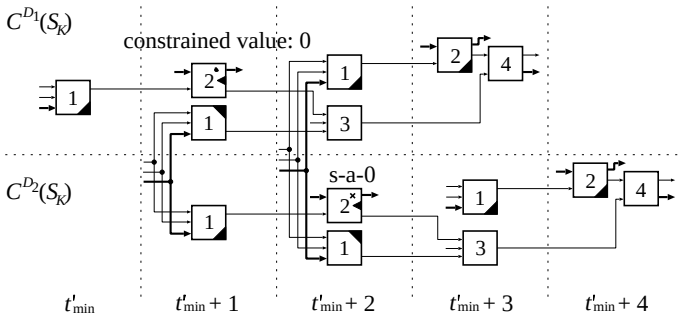

Fig. 4. Double time-expansion model of Fig. 2: $C^D(S_K)$

Definition 1. *Let S be an acyclic sequential circuit, and $C^T(S)$ be a TEM of S. Then, a combinational circuit obtained by the following procedure is said to be a double time-expansion model (DTEM) $C^D(S)$ of S.*

Step 1: *Make two copies of $C^T(S)$: $C^{D_1}(S)$, $C^{D_2}(S)$.*
Step 2: *Connect each pair of PIs u in $C^{D_1}(S)$ and v in $C^{D_2}(S)$ such that $t(u) - t(v) = 1$ and $l(u) = l(v)$, and feed a new primary input w into them, where $l(u) = l(v)$ means that u and v are identical in S.* □

According to the above definition, a DTEM $C^D(S_K)$ of S_K (Fig. 2) is constructed as Fig. 4. Note that, although two copies of CLB 1 in $t'_{\min}+1$ (also in $t'_{\min}+2$) can be merged into one CLB, $C^D(S_K)$ is expressed as Fig. 4 to differentiate $C^{D_1}(S_K)$ and $C^{D_2}(S_K)$ from each other. If one wants to test the slow-to-rise fault on line l in S_K, test generation for one of the corresponding stuck-at 0 fault is performed on $C^D(S_K)$ under the constrained value of 0 that must be satisfied during test generation. In this way, transition tests for an acyclic sequential circuit can be generated by using a DTEM.

In [9], an acyclic sequential circuit is assumed to be obtained as a kernel circuit of a given circuit by using enhanced scan technique. Thereby, two consecutive vectors V_1 and V_2 to be applied to PPIs at the times corresponding to $t'_{\min}+1$ and $t'_{\min}+2$ in Fig. 4 can be stored in ESFFs. Here, suppose a given circuit is designed by using standard scan technique. In this case, V_1 and V_2 for PPIs cannot be stored in SFFs but only V_1 can be stored. Consequently, V_2 must be justified by using some technique. In the next section, we discuss this problem.

3 Proposed Method

3.1 Broadside Test Generation Model

As explained in Sect. 2.2, in a DTEM, vectors for PPIs in a frame where a stuck-at fault exists must be justified by using some technique. Note that this

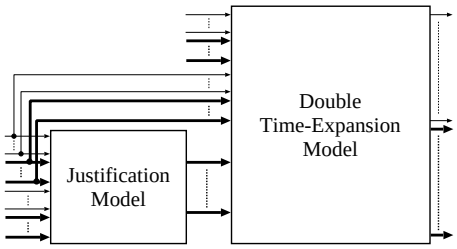

Fig. 5. Sketch of a broadside test generation model

frame is called a test frame. To achieve this requirement, we propose a new test generation model called a broadside test generation model. The sketch of a broadside test generation model is shown in Fig. 5. A broadside test generation model is composed of a DTEM and a justification model which is used for the above requirement. We first define a justification model as follows.

Definition 2. *Let S and S_K be a partial scan circuit and its acyclic kernel circuit, respectively. Let $C^T(S_K)$ and $C^D(S_K)$ be a TEM of S_K and a DTEM of S_K, respectively. Let t be the label value of a test frame in $C^D(S_K)$. Then, a combinational circuit obtained by performing the following procedure is said to be the justification model (JM) $C_t^J(S_K)$ with respect to t.*

Step 1: *For each PPI which belongs to only $C^{D_2}(S_K)$ in t, extract the logic cone of the corresponding PPO in $C^T(S_K)$. Also, for each PPI shared by $C^{D_1}(S_K)$ and $C^{D_2}(S_K)$ in t, extract the logic cone of the corresponding PPO in $C^T(S_K)$.*

Step 2: *For each pair of the logic cones, connect each pair of PIs (resp. PPIs) u in one cone and v in the other cone such that $t(u) = t(v)$ and $l(u) = l(v)$, and feed a new PI (resp. PPI) w into them.* □

By using a JM and a DTEM, a broadside test generation model is defined as follows.

Definition 3. *Let S and S_K be a partial scan circuit and its acyclic kernel circuit, respectively. Let $C^D(S_K)$ and $C_t^J(S_K)$ be a DTEM of S_K and the JM with respect to the label value t of a test frame in $C^D(S_K)$. Then, a combinational circuit obtained by performing the following procedure is said to be the broadside test generation model (BTGM) $C_t^B(S_K)$ with respect to t.*

Step 1: *For each PPI which belongs to only $C^{D_2}(S_K)$ in t, connect the corresponding PPO of $C_t^J(S_K)$ to the PPI. Also, for each PPI shared by $C^{D_1}(S_K)$ and $C^{D_2}(S_K)$ in t, connect the corresponding PPO of $C_t^J(S_K)$ to the PPI.*

Step 2: *Connect each pair of PIs (resp. PPIs) u in $C_t^J(S_K)$ and v in $C^D(S_K)$ that $t(u) = t(v)$ and $l(u) = l(v)$, and feed a new PI (resp. PPI) w into them.* □

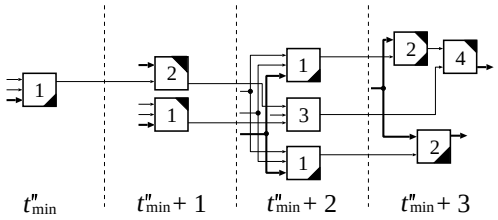

Fig. 6. Justification model with respect to $t'_{\min}+2$ in Fig. 4: $C^J_{t'_{\min}+2}(S_K)$

Notice that, for a given circuit, $d+1$ JMs are created, where d denotes the sequential depth of its kernel circuit. Hence, $d+1$ BTGMs are also created.

Figure 6 shows the JM $C^J_{t'_{\min}+2}(S_K)$ of Fig. 4. This JM is composed of the logic cone of the PPO of CLB 4 in $t_{\min}+3$ (Fig. 3) and that of the PPO of CLB 2 in $t_{\min}+3$. Note that although those two logic cones can share CLBs 1 and 2, we explicitely express the two logic cones for simplicity. Figure 7 shows the BTGM $C^B_4(S_K)$ of Fig. 4. In creating this BTGM, the value of 2 is assigned to $t'_{\min}$ of Fig. 4 and the value of 0 is assigned to $t''_{\min}$ of Fig. 6. As shown in Fig. 7, CLBs in a frame are not shared to differentiate the DTEM and the JM. Patterns that are needed to activate stuck-at faults in a test frame and propagate those effects to a PO or a PPO can be justified by using its JM.

3.2 Test Generation Procedure

Given a partial scan circuit S whose kernel circuit S_K is acyclic, broadside transition tests for S are generated as follows.

Step 1: Create a transition fault list F^T of S.
Step 2: Construct $d+1$ BTGMs $C^B_{t_1}(S_K), \ldots, C^B_{t_{d+1}}(S_K)$ of S_K, where d is the sequential depth of S_K.
Step 3: Create stuck-at fault lists F^S_1 for $C^B_{t_1}(S_K)$, ..., F^S_{d+1} for $C^B_{t_{d+1}}(S_K)$ corresponding to F^T, and constrained value lists C_1 for F^S_1 , ..., C_{d+1} for F^S_{d+1}.
Step 4: For each stuck-at fault $f^S \in F^S_i$ $(i = 1, \ldots, d+1)$,
(a): generate a test pattern t^S under the corresponding constraint $c \in C_i$, and
(b): transform t^S into a broadside test t^T for the corresponding transition fault $f^T \in F^T$ according to the label information of $C^B_{t_i}(S_K)$.

Note that, in Step 3, even if a transition fault in a given circuit corresponds to some stuck-at faults in its BTGMs, we can handle the respective stuck-at faults one by one. This is because generated broadside transition tests are applied in the slow-fast-slow testing manner. In Step 4, if all the stuck-at faults corresponding to a transition fault are identified as untestable, the transition

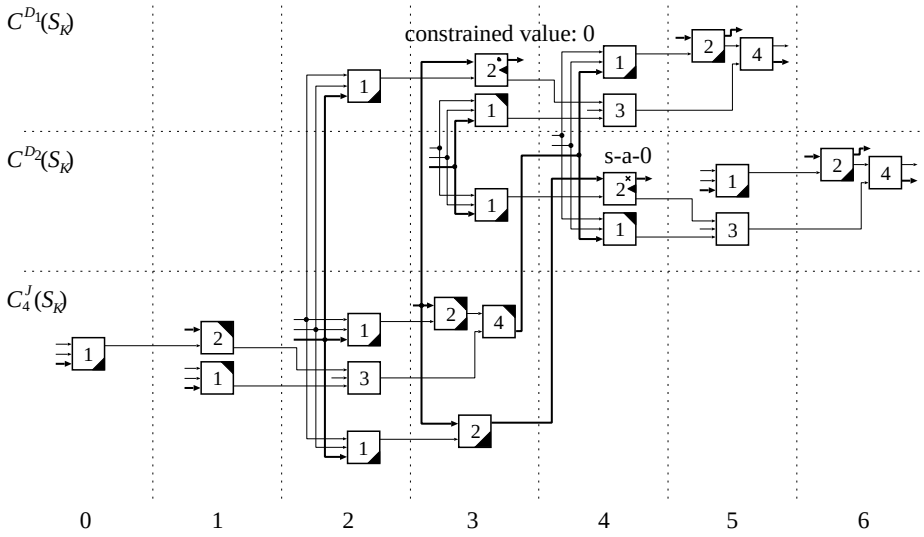

Fig. 7. Broadside test generation model with respect to $t'_{\min} + 2$ ($t'_{\min} = 2$) in Fig. 4: $C_4^B(S_K)$

fault is also untestable. Furthermore, it is sufficient to generate a test pattern for one of the stuck-at faults corresponding to a transition fault. In Step 4 (b), t^S is transformed into t^T as follows. For example, in Fig. 7, a pattern for each of the PIs and the PPI of CLB 1 in frame 0 is transformed into a pattern for each of the PIs of CLB 1 and the corresponding SFF at time 0 in Fig. 2. Notice that, the pattern for the SFF is set by scan-in operation before time 0. Other patterns in frames from 1 to 6 are transformed in the same way.

The following theorem guarantees the correctness of our test generation method.

Theorem 1. *Let S and S_K be a partial scan circuit and its kernel circuit which is acyclic, respectively. Let $f_\uparrow^T$ (resp. $f_\downarrow^T$) be a slow-to-rise (resp. slow-to-fall) transition fault in S. Let $F_{s\text{-}a\text{-}0}^S$ (resp. $F_{s\text{-}a\text{-}1}^S$) be the set of stuck-at 0 (resp. 1) faults corresponding to $f_\uparrow^T$ (resp. $f_\downarrow^T$). Then, $f_\uparrow^T$ (resp. $f_\downarrow^T$) is testable under the broadside testing manner if and only if at least one $f_{s\text{-}a\text{-}0}^S \in F_{s\text{-}a\text{-}0}^S$ (resp. $f_{s\text{-}a\text{-}1}^S \in F_{s\text{-}a\text{-}1}^S$) in the corresponding BTGM $C_t^B(S_K)$ is testable under the constrained value of 0 (resp. 1).*

Proof. Broadside test generation for $f_\uparrow^T$ (resp. $f_\downarrow^T$) in S can be viewed as test generation for the stuck-at 0 (resp. 1) fault in S corresponding to $f_\uparrow^T$ (resp. $f_\downarrow^T$) in a situation where (a) the constrained value of 0 (resp. 1) has to be set to the faulty site at time $t_{1\text{st}}$, and (b) no scan operation has to be performed between $t_{1\text{st}}$ and $t_{2\text{nd}}$. Here, $t_{2\text{nd}}$ denotes a time at which the stuck-at 0 (resp. 1) fault in S is activated, and $t_{1\text{st}} = t_{2\text{nd}} - 1$. In [8], it has been shown that the stuck-at

test generation problem for an acyclic sequential circuit can be reduced to that for its TEM. The properties of a TEM still hold in a BTGM because the BTGM is constructed by using the TEM. Hence, to demonstrate this theorem, we need to show that (a) and (b) are satisfied in test generation for the BTGM.

First, under the slow-fast-slow testing manner, it is sufficient to consider whether at least one $f^S_{\text{s-a-0}} \in F^S_{\text{s-a-0}}$ (resp. $f^S_{\text{s-a-1}} \in F^S_{\text{s-a-1}}$) is testable. Since, in $C^B_t(S_K)$, stuck-at test generation for $f^S_{\text{s-a-0}}$ (resp. $f^S_{\text{s-a-1}}$) is performed under the constrained value of 0 (resp. 1), (a) is satisfied. Furthermore, since patterns for $f^S_{\text{s-a-0}}$ (resp. $f^S_{\text{s-a-1}}$) in the test frame of $C^B_t(S_K)$ are justified by its JM, (b) is also satisfied. Thus, the theorem is demonstrated. □

3.3 Test Application

This subsection describes how to apply broadside transition tests to a partial scan circuit.

Broadside transition tests generated by the method of Sect. 3.2 are applied to a partial scan circuit S whose kernel circuit S_K is acyclic as follows. Let $C^D(S_K)$ be a DTEM of S_K, and t be the label value of a test frame. In test application, the circuit is operated at a slow clock speed except when its rated clock is applied at the time corresponding to t. If there exists a PPI in a frame before the test frame, scan-in operation is performed before the corresponding time. Also, if there exists a PPI which belongs to only $C^{D_2}(S_K)$ in a frame after the test frame t, scan-in operation is performed before the corresponding time. Scan-out operation is performed after the corresponding time if there exists a PPO which belongs to only $C^{D_2}(S_K)$ in a frame between the test frame t and the last frame. Note that, in order to keep the values of normal FFs during scan operation, the system clock must be separated from the scan clock or all the normal FFs have to be redesigned such that the values can be held during scan operation. For example, a broadside transition test generated by performing test generation on the BTGM $C^B_4(S_K)$ shown in Fig. 7 is applied to the partial scan circuit shown in Fig. 1 as follows. Scan-in operation is performed before each time from 0 to 3, then the circuit is operated at a slow clock speed. The transition to activate a fault is created between times 3 and 4, then between times 4 and 5, its fault effect is captured at the rated clock speed. Before each time of 5 and 6, scan-in and scan-out operations are performed simultaneously, then the circuit is operated at the slow clock speed. After time 6, scan-out operation is performed. Let d be the sequential depth of S_K. The length of a broadside transition test can range from $d + 2$ to $2d + 2$. In the case of Fig. 2, it ranges from 5 to 8.

3.4 Experimental Results

Here, we evaluate the proposed method in terms of area overhead, fault coverage, fault efficiency and test generation time.

The following experiment was performed on a Sun Fire V890 workstation (CPU: UltraSPARC IV 1.35GHz × 8, Memory: 64GB). TetraMAX from Synopsys was used as a stuck-at test generation tool, and its backtrack limit was set to

Table 1. Circuit characteristics

Circuit	#PIs	#POs	#FFs	Area
EWF	57	32	352	9,276
IIR	48	32	224	16,519
JWF	44	32	224	6,947
LWF	35	32	96	2,614
Paulin	41	64	192	19,174
Tseng	104	32	160	12,150

Table 2. Area overheads

Circuit	Area OH [%]		
	ES	SS	Ours
EWF	64.5	26.6	16.9
IIR	23.1	9.5	5.4
JWF	54.8	22.6	16.1
LWF	62.4	25.7	8.6
Paulin	17.0	7.0	4.7
Tseng	22.4	9.2	3.7

100. We applied our method to six 32bit datapath circuits [16]. The characteristics of the circuits are shown in Table 1. Columns "#PIs," "#POs" and "#FFs" list the number of PIs, POs and FFs, respectively. Column "Area" gives the area of a circuit which is estimated by Design Compiler from Synopsys, where the area of a 2-input NAND gate is considered to be 2. In this experiment, we compared the proposed method to fully enhanced scan testing and broadside testing based on the full scan method.

We first show area overheads needed for the three methods considered. In our method, acyclic kernel circuits for all the circuits were obtained by using the exact algorithm in [4]. Table 2 lists area overheads. In the table, fully enhanced scan testing, broadside testing based on the full scan method and the proposed one are denoted by "ES," "SS" and "Ours," respectively. In estimating area overhead, the areas of an ESFF and an SFF were 27 and 17, respectively. For all the circuits, we achieved the lowest area overheads. Since the proposed method is based on partial scan design, we can achieve low area overhead compared with the other methods.

Next, we show test generation results. In this experiment, we compared fault coverage, fault efficiency and test generation time of our method with those of the other two methods, and fault simulation was not invoked. In "ES," to generate transition tests, constrained stuck-at test generation were performed on a combinational circuit that consists of two independent copies of the combinational part of a given circuit. For example, to generate a two-pattern test for a slow-to-rise transition fault, we performed stuck-at test generation for the stuck-

Table 3. Test generation results

Circuit	Method	#flts	FC [%]	FE [%]	TGT [s]	Model Size
EWF	ES	17,646	99.86	100.00	27.69	11,512
	SS		99.86	100.00	23.34	11,512
	Ours		99.86	100.00	32.62	26,268
IIR	ES	38,444	99.85	100.00	106.31	28,558
	SS		99.85	100.00	104.27	28,558
	Ours		99.85	100.00	229.43	83,574
JWF	ES	13,692	99.88	100.00	15.76	9,414
	SS		99.88	100.00	14.65	9,414
	Ours		99.88	100.00	14.35	16,788
LWF	ES	4,804	99.83	100.00	3.51	3,308
	SS		99.81	100.00	3.64	3,308
	Ours		99.81	100.00	2.77	6,171
Paulin	ES	46,248	100.00	100.00	165.33	34,508
	SS		100.00	100.00	164.12	34,508
	Ours		100.00	100.00	252.15	51,762
Tseng	ES	28,592	100.00	100.00	83.07	21,100
	SS		99.68	100.00	101.81	21,100
	Ours		99.68	100.00	154.58	33,051

at 0 fault in the second copy under the following constraint: the value of 0 must be set to the corresponding site in the first copy. Similarly, in "SS," we performed constrained stuck-at test generation on a combinational circuit corresponding to the two time frames of a given circuit. For example, to generate a two-pattern test for a slow-to-rise transition fault, we performed stuck-at test generation for the stuck-at 0 fault in the second time frame under the following constraint: the value of 0 must be set to the corresponding site in the first time frame. Table 3 lists the test generation results. Column "#flts" represents the number of targeted transition faults. Columns "FC [%]," "FE [%]" and "TGT [s]" denote fault coverage, fault efficiency and test generation time, respectively. The last column "Model Size" represents the average area of broadside test generation models in "Ours," and the area of the test generation model used in each case of "ES" and "SS," which are estimated by Design Compiler. In Table 3, all the methods achieved complete fault efficiency. However, in the case of "LWF" and "Tseng," some untestable faults in "SS" and "Ours" were unintentionally detected in "ES." Thus, in terms of over-testing, "ES" is not desirable. Since our broadside test generation model is larger (about 2.0 times larger on average) than the test generation models used in the other two methods, the test generation time of our method increased in some circuits. However, we consider our method to be comparable to the other two methods in test generation time. The reason is as follows. In [19], the time complexity for practical instances of the test generation problem for combinational circuits was claimed to be $O(n^3)$, where n is the size of a combinational circuit. Nevertheless, it was not observed

in our method. For example, in "IIR," the test generation time of our method was only about 2.2 times longer than that of the other two methods, although the size of our broadside test generation model was about 2.9 times larger than that of the test generation models used in the other two methods.

From the above results, we can see that our method can provide a good trade-off between area overhead and test generation effort. It is conceivable that the proposed method can also work efficiently for more complex circuits because combinational stuck-at test generation is performed.

4 Variations of Broadside Transition Testing of Partial Scan Circuits

4.1 Two Test Application Strategies

As mentioned in Sect. 2.1, the scan-per-vector strategy or the scan-per-test strategy can be used during test application. By using the iterative array model [3] of a partial scan circuit, the two test application strategies can be represented as Fig. 8. In Fig. 8, each box represents the combinational part of the partial scan circuit. In the case of the scan-per-vector strategy, inputs (resp. outputs) corresponding to SFFs shown in Fig. 8(a) are considered to be primary inputs (resp. primary outputs) except in the fault activation phase. For the stuck-at $c \in \{0, 1\}$ fault in the iterative array model of Fig. 8(a), a test pattern which detects the stuck-at fault with satisfying the constrained value of c is equivalent to a broadside test for the corresponding transition fault. Since we consider a partial scan circuit whose kernel circuit is acyclic, the fault initialization and fault effect propagation phases are bounded. Therefore, the length of a broadside transition test is at most $2d + 2$ where d is the sequential depth of the kernel circuit. Indeed, our test generation model proposed in Sect. 3.1 can be interpreted as a compact and sophisticated model of the iterative array model.

In the case of the scan-per-test strategy, inputs (resp. outputs) corresponding to SFFs shown in Fig. 8(b) are considered to be primary inputs (resp. primary outputs) only in the first time frame (resp. last time frame). This test application strategy has some advantages against the scan-per-vector strategy. Since few scan operations are required compared to the scan-per-vector strategy, the scan-per-test strategy is effective in test application time. Furthermore, overtesting can be alleviated compared to the scan-per-vector strategy, because the circuit behavior under the scan-per-test strategy is more similar to the original circuit behavior than that under the scan-per-vector strategy. Clearly, the set of untestable transition faults under the scan-per-test strategy is a superset of the set of untestable transition faults under the scan-per-vector strategy. It is notable that, unlike the scan-per-vector strategy, there are no restrictions on the scan clock and the normal FFs in the scan-per-test strategy. Thus, since the scan-per-test strategy has some desirable properties, an efficient method to generate broadside transition tests under the scan-per-test strategy should also be investigated in the future.

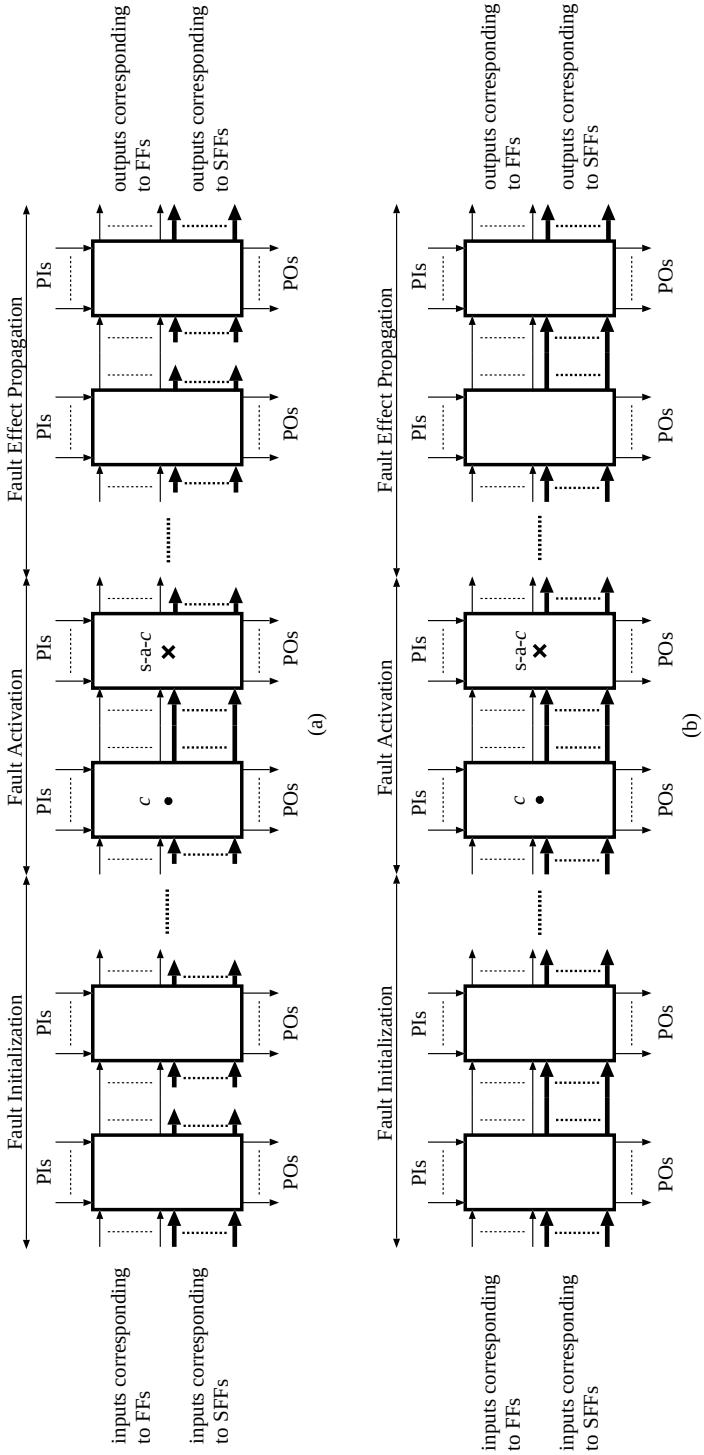

Fig. 8. Two test application strategies: (a) scan-per-vector and (b) scan-per-test

4.2 Fault Sizes

In this work, we only target transition faults whose sizes are one. However, it is important to consider fault sizes during test generation to detect large delay defects. Here we mention how to detect transition faults whose sizes are more than one in a partial scan environment.

In [21], transition faults whose sizes are more than one in a full scan circuit were handled. The basic idea used in [21] can easily be adapted to partial scan circuits. Again, we use the iterative array model of a partial scan circuit to explain how transition faults whose sizes are more than one are handled. Figure 9 shows the iterative array models under the scan-per-vector and scan-per-test strategies to generate a broadside test for a transition fault whose size is more than one. For the stuck-at $c \in \{0, 1\}$ fault in Fig. 9(a) (also (b)), a test pattern which detects the stuck-at fault with satisfying the constrained values of $c, \bar{c}, \ldots, \bar{c}$ corresponds to a broadside test for the corresponding transition fault whose size is more than one. For example, in the case of a slow-to-rise fault whose size is three, four clock cycles are required to activate the transition fault. In the iterative array model, a test pattern for the corresponding stack-at 0 fault sets the constrained values of $0, 1, 1$ to the time frames corresponding to the fault activation phase. In this way, transition faults whose sizes are more than one can be handled for partial scan circuits. However, a more precise analysis will be needed in future work.

5 Conclusions and Future Work

In this paper, we investigated broadside transition testing of partial scan circuits. The proposed scheme can utilize existing combinational stuck-at test generation tools to generate broadside transition tests. From a practical point of view, this feature is very useful because existing techniques for combinational stuck-at test generation reach a mature level. Through experiments, we showed that our method can reduce area overhead and can generate broadside transition tests in reasonable test generation time.

As mentioned in Sect. 4, broadside transition testing of partial scan circuits under the scan-per-test strategy should be investigated in the future. Moreover, fault sizes should be taken into account in future work. We also plan to extend the proposed method so that the path delay fault model can be handled.

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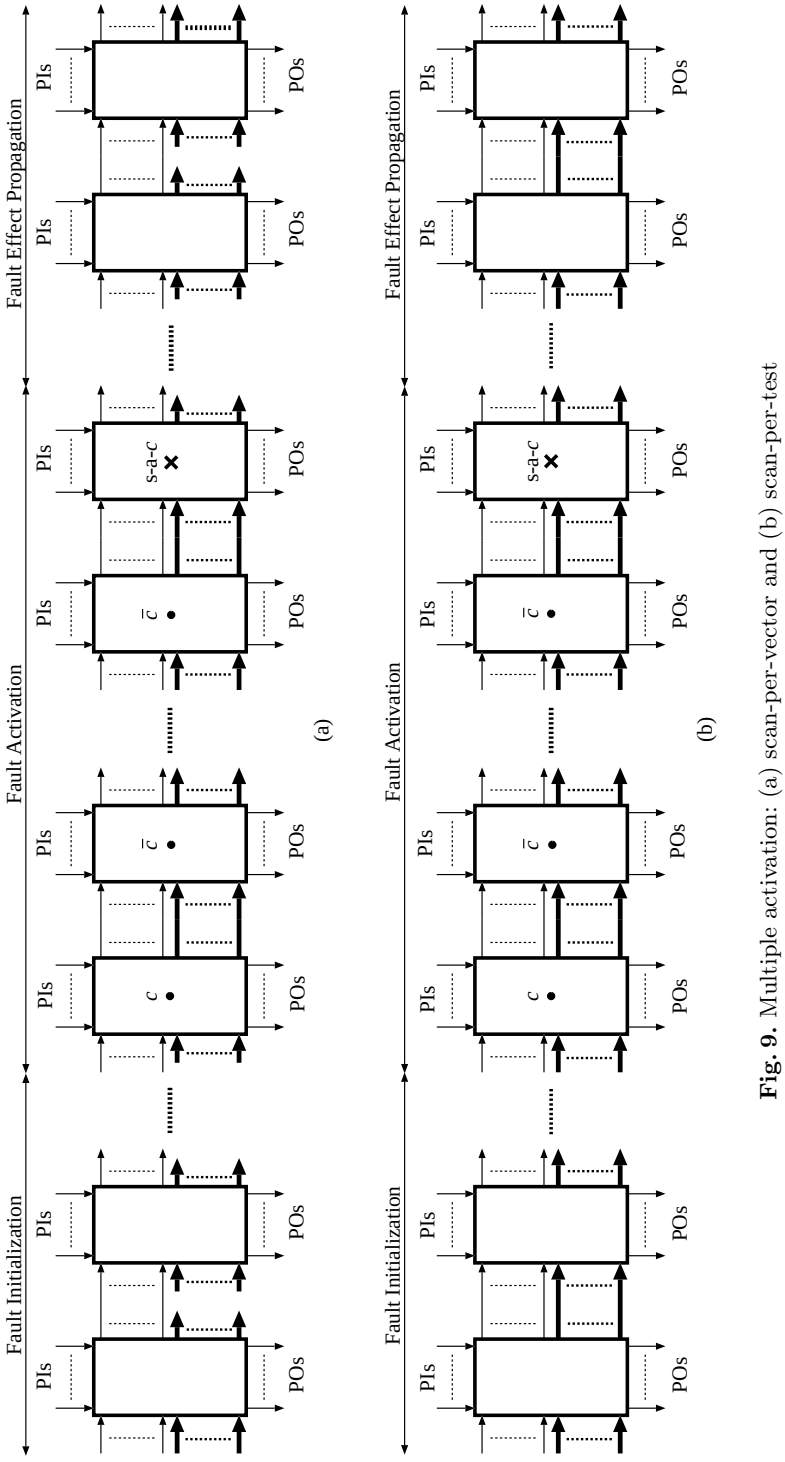

Fig. 9. Multiple activation: (a) scan-per-vector and (b) scan-per-test

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