# CAT platform for analogue and mixed-signal test evaluation and optimization*

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**Abstract.** This paper introduces a Computer-Aided-Test platform that has been developed for the evaluation of test techniques for analogue and mixed-signal circuits. The CAT platform, integrated in the Cadence Design Framework Environment, includes tools for fault simulation, test generation and test optimization for these types of circuits. Fault modeling and fault injection are simulator independent, which makes this approach flexible with respect to past approaches. In this paper, the use of this platform is illustrated for test optimization for the case of a fully differential amplifier. Test limits are set using a statistical circuit performance analysis that accounts for process deviations, as a trade-off between estimated test metrics at the design stage. Specification-based tests are next optimized in terms of their capability of detecting catastrophic and parametric faults.

## 1 Introduction

The test of integrated analogue and mixed-signal circuits differs importantly from the test of digital circuits. The major difference stems from the need to consider continuous signals and circuit parametric deviations, in addition to just catastrophic faults (opens and shorts). For digital circuits, structural testing has provided cost efficient solutions that target the test of catastrophic faults rather than the test of the circuit functionality. Thus, fault coverage is the major test metric in this domain and is somehow independent from the specifications. For analogue circuits, the need to consider parametric deviations has lead to the definition of analogue test metrics that take into account also the circuit functionality. In other words, even when a parametric fault-based test approach is considered for analogue circuits, test metrics such as fault coverage cannot be calculated without knowing the performance specifications [1].

*This research work was supported by European MEDEA+ program under the project NanoTEST-2A702.

The domain of integrated analogue and mixed-signal testing has always tried to cope with a controversy between functional and structural testing. Functional testing is practically always considered but research on structural testing continue to make progress. In fact, it has appeared clear for some test users that to find manufacturing faults such as shorts, opens and misloaded components in mixed-signal circuits is essential, and this comforted the proposal of the IEEE 1149.4 Analogue Boundary-scan mixed-signal test architecture [2]. Also, it has been shown that the study of catastrophic faults helps in identifying reliability problems in mixed-signal circuits, in particular redundant components [3]. In general, since it is possible to define a fault list for catastrophic faults, the study of catastrophic faults helps also for the generation and optimization of test patterns, even under the presence of process deviations [4].

The case of parametric faults has been considered by many authors by simply modifying the nominal values of a design parameter, and considering Monte Carlo simulations. In this way, parametric fault lists have been built in a rather arbitrary way. Recently, [1] introduced a different way of defining parametric faults. A parametric fault is considered as the minimum deviation of a design parameter that results in a circuit specification being violated. In this approach, parametric faults are obtained by transient simulations, without recurring to time consuming Monte Carlo simulations. This approach is quite acceptable when faults are considered the result of a single parameter deviation, while the other parameters remain at their nominal values. However, it cannot deal properly with the case of device misbehaviour resulting from the combination of multiple small deviations.

An early approach to avoid Monte Carlo simulation was based on the use of sensitivity analysis to deterministically identify the bounds on circuit parameters [5]. Process information and the sensitivity of the circuit principal components have been recently considered in [6] for generating the statistical models of the fault-free and faulty circuits, which is then used for test vector generation. These models are obtained using a statistical approach and a linear estimation, rather than Monte Carlo simulations. Another statistical approach is considered in [7]. Here, however, parametric faults are injected by swapping transistors, one at a time, by a transistor whose process parameters are shifted by $3\sigma$ and a sensitivity analysis is performed only in the DC domain. The problem with these approaches is again that the misbehaviour resulting from the combination of multiple small deviations cannot be evaluated properly.

In this work, we will introduce a Computer-Aided-Test platform for analogue and mixed-signal circuits. The CAT platform, integrated in the Cadence Design Framework Environment, includes tools for fault simulation, test generation and test optimization. Aspects on fault simulation and test optimization will be illustrated in this paper for the case of a fully differential amplifier. We will consider a statistical analysis that is based on Monte Carlo simulations. This analysis will allow the calculation of analogue test metrics under process deviations, and this will be used for setting test limits. These test limits will then be used for the evaluation of test metrics under catastrophic and parametric faults.

Specification-base tests will then be optimized according to fault coverage for a fully differential amplifier.

## 2 The CAT platform

### 2.1 Architecture of the platform

Figure 1 shows a simplified architecture of the proposed CAT platform. It is composed of three separate tool sets. Fault modelling, fault injection and fault simulation are carried out using the tool set FIDESIM. The results are saved in a database that can be read by the other tool sets, in particular the OPTEVAL tool set for test evaluation and the OPTEGEN tool set for test generation.

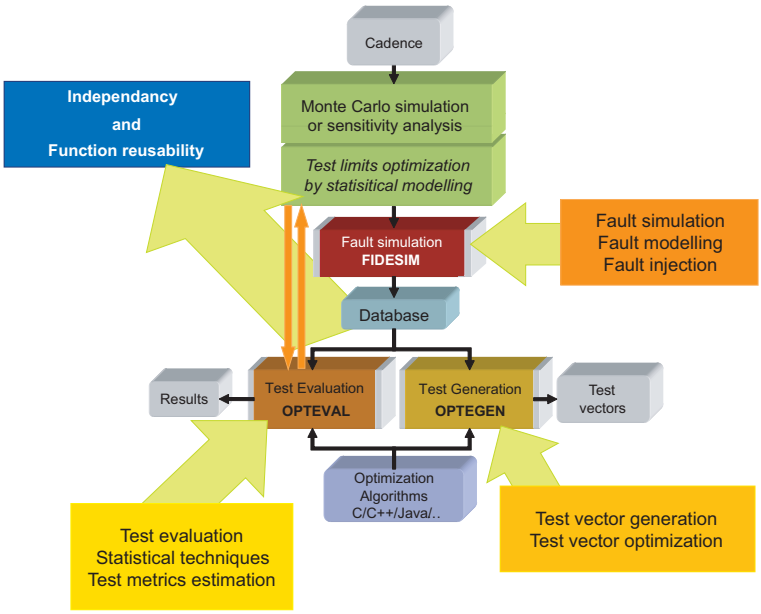



**Fig. 1.** Simplified architecture of the CAT platform.

In this paper, we will illustrate the use of the FIDESIM and OPTEVAL tool sets. The tool set OPTEGEN is the subject of further work. It currently includes three tools. The first tool is used for compaction of analogue functional tests. A second tool is used for the generation of multi-frequency test sets using the fault-based test approach described in [8]. This technique is valid for linear time-invariant circuits and allows the generation of a minimal set of test vectors for maximum fault coverage and, if required, maximal diagnosis. A third tool is available for the coding of analogue test patterns as optimized bit streams, as described in [9], following an approach first presented by [10].

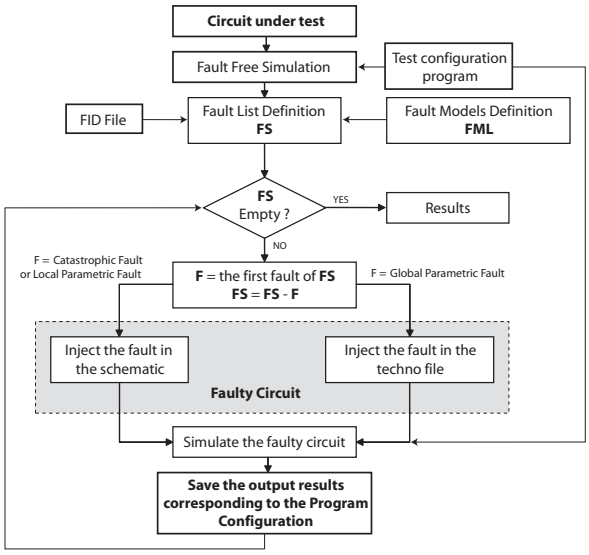
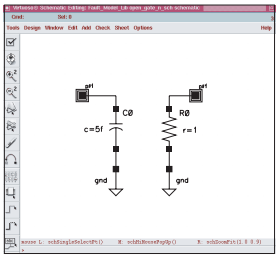



**Fig. 2.** Fault simulation procedure used by FIDESIM.

### 2.2 Fault modeling and fault injection tools

Several tools for analogue fault modelling, fault injection and fault simulation have appeared in the literature. Most of these tools are in-house developments. For example, in [7] a fault simulator called DOTTS is used for both catastrophic and parametric faults under process variations. It is also being considered for RF circuits [12, 13]. Catastrophic faults under process variations are considered by the ANTICS fault simulation environment [4]. Another in-house development called SWITTEST has been presented for fault simulation of parametric and catastrophic faults in switched capacitor systems [14]. A commercial tool for parametric fault simulation and test vector generation exploiting sensitivity analysis and statistical modelling has been commercialised [6]. Several other tools have been developed, especially for academic research, and it is not our aim to describe all of them. The common point of all these tools is that they modify the netlist of the circuit to perform the fault injection in a way that is dependent on the simulator netlist under use.

However, [15] presents a tool where the fault models are added, before simulation, in the schematic of the design (in Cadence®), and the faults are injected by changing the parameters of each fault model. The injection of fault models into the circuit schematics is also considered in the tool described in [16]. The netlist for fault simulation is then generated after the schematics, and thus can be independent of the simulator under use. The fault simulation tool set FIDESIM is based on this earlier development. A detailed description of fault model building and fault injection is given in [16]. The Fault simulation procedure is shown in Figure 2.




(a)

```
(((1 "Fault_Model_Lib" "gateOpenN"))
(((1 (4) ("inst" "tran" ("M1" "M2"))
(nil 1 2) ))))
```

(b)

**Fig. 3.** Description of a fault model: (a) fault model, and (b) fault injection description file.

```
SPECIFICATIONS
pr1:(70,85)
TC_TOLERANCES
tc1:(200M,260M)
OUTPUTS
tm1 = dB20(VF("/out1")-VF("/out2"))
tm2 = phase(VF("/out1")-VF("/out2"))
PERFORMANCES
pr1 = value(tm1 100)
TEST_CRITERIA
tc1 = root(tm2 0 1)
```

**Fig. 4.** Test Program example.

The test engineer designs a set of fault models under the Cadence® DFII (Design Framework II) environment. A fault model is saved in a library just as a Cadence cellview. These fault models must observe some rules to allow the automatic fault injection, in particular relating to the pinout. Thus, for each fault model, the injection procedure is described using a pseudo code called FID (Fault Injection Description) stored in a file. Local, and global parametric faults can be considered as well. For example, Figure 3(a) describes the circuit that corresponds to an open in an NMOS transistor gate. The FID file for describing an injection of this fault is shown in Figure 3(b). This fault model is a cellview stored in the library "Fault_Model_Lib".

The different test benches for the circuit under test (CUT), the calculation of the circuit performances and the calculation of the proposed test measurements or test criteria are described as a pseudo code called *Test Configuration*. Figure 4 shows an example of this where one performance, two test measures and one test criteria are defined. The test measures are used to define the performances and the test criteria on which a tolerance test threshold is given.

The CUT may require several test benches and different types of analysis to measure its performances and test criteria. Thus, it generally needs to be simulated in multiple test benches under the same fault injection. FIDESIM

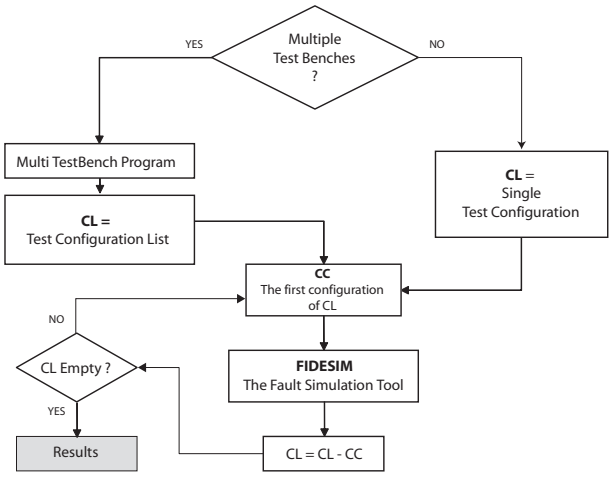



**Fig. 5.** Architecture of the multiple testbench procedure.

is able to perform this by describing the different test benches in the form of a pseudo code called *Multi TestBench Program*. This is illustrated by the procedure shown in Figure 5. This feature will be specially important during Monte Carlo simulations, since an instance generated during Monte Carlo will be simulated for all different test benches, before proceeding with the next instance.

## 3 Test metrics estimation

The test evaluation and optimization tool set OPTEVAL is developed to evaluate test techniques by estimating analogue test metrics. The estimation of test metrics such as defect level, test yield or yield loss is important in order to quantify the quality and cost of a test approach. For design-for-test purposes (DFT), this is important in order to select the best test measurements but this must be done at the design stage, before production test data is made available. In the analogue domain, previous works have considered the estimation of these metrics for the case of single faults, either catastrophic or parametric. The consideration of single parametric faults is sensible for a production test technique if the design is robust. However, in the case that production test limits are tight, test escapes resulting from multiple parametric deviations may become important. In addition, aging mechanisms result in field failures that are often caused by multiple parametric deviations. In the CAT platform presented here, we will consider the estimation of analogue test metrics under the presence of multiple parametric deviations (or process deviations) and under the presence of faults. A statistical model of a circuit is used for setting test limits under process deviations as a trade-off between test metrics calculated at the design stage. This model is obtained from a Monte Carlo circuit simulation, assuming Gaussian Probability Density Functions (PDFs) for the parameter and performance deviations.

After setting the test limits considering process deviations, the test metrics are calculated under the presence of catastrophic and parametric single faults for different potential test measurements. We will illustrate the technique for the case of a fully differential operational amplifier, proving the validity in the case of this circuit of the Gaussian PDF.

### 3.1 Definition of test metrics

The test metrics considered for analogue circuits are [1]: Yield $Y$, Test Yield $Y_T$, Yield Coverage $Y_C$, Yield Loss $Y_L$, Defect Level $D$ and Fault Coverage $F$ where:

$$\begin{aligned} Y &= \text{Proportion of the functional (or good) circuits} \\ &= P(\text{circuit is functional}) \\ Y_T &= \text{Proportion of the circuits that pass the test} \\ &= P(\text{circuit passes the test}) \\ Y_C &= \text{Proportion of the pass circuits that are functional} \\ &= P(\text{circuit passes the test/is functional}) \\ Y_L &= \text{Proportion of the fail circuits that are functional} \\ &= 1 - Y_C \\ D &= \text{Proportion of the faulty circuits that pass the test} \\ &= 1 - P(\text{circuit is functional/passes the test}) \end{aligned}$$

where a functional (or good) circuit is the one for which all its performances are inside their specifications and a faulty circuit is the one for which at least one of its specifications is violated.

The definition of parametric fault coverage will be detailed later. For catastrophic faults, as mentioned earlier, device functionality is not considered and fault coverage is just defined as the ratio of detected faults with respect to the total number of injected faults.

### 3.2 Test metrics theoretical computation

Assume that we have $n$ performances and $m$ test criteria. Let $A = (A_1, \cdots, A_n)$ be the set of the specifications of the performances and $B = (B_1, \cdots, B_m)$ the test limits (intervals of the accepted values of the test criteria). The test metrics are then calculated theoretically as follows:

$$Y = \int_A f_S(s)\ ds \tag{1}$$

$$Y_T = \int_B f_T(t)\ dt \tag{2}$$

$$Y_C = \frac{\int_A \int_B f_{ST}(s,t)\ ds\ dt}{Y} \tag{3}$$

$$D = 1 - \frac{\int_A \int_B f_{ST}(s,t)\ ds\ dt}{Y_T} \tag{4}$$

where, $f_S(s) = f_S(s_1, s_2, \cdots, s_n)$ is the joint probability density of the performances, $f_T(t) = f_T(t_1, t_2, \cdots, t_m)$ is the joint probability density of the test criteria and $f_{ST}(s,t) = f_{ST}(s_1, s_2, \cdots, s_n, t_1, t_2, \cdots, t_m)$ is the joint probability density of the performances and the test criteria.

For the case of catastrophic faults, fault coverage is the major metric and this can be readily computed. For the case of single parametric faults, for which a fault list is available, test metrics can be computed following, for example, the technique described in [1]. However, the analysis of faulty behaviour resulting from process deviations (multiple small parametric deviations) has not been properly studied in the past, since it is impossible to produce an actual fault list. We will next describe the statistical analysis performed in the tool set for evaluating test metrics and setting test limits under process deviations. The use of these tools will be illustrated later for the case of a test vehicle.

### 3.3 Test metrics computation under process deviations

Given a vector $X = (X_1, X_2, ..., X_p)^T$ composed of random variables, where $X_j$ for $j = 1, 2, ..., p$, is a one-dimensional random variable, the covariance of $X_i$ and $X_j$ is a measure of dependency between these random variables and is defined by:

$$\nu_{X_i X_j} = Cov(X_i, X_j) = E(X_i X_j) - E(X_i)E(X_j) \tag{5}$$

where $E(.)$ denotes the expected value. If $X_i$ and $X_j$ are independent of each other, the covariance $\nu_{X_i X_j}$ is necessarily equal to zero. The converse is not true. The covariance of a random variable $X_i$ with itself is the variance:

$$\nu_{X_i X_i} = Cov(X_i, X_i) = \nu_{X_i} \tag{6}$$

The correlation between two variables $X_i$ and $X_j$ is defined from the covariance as follows:

$$\rho_{X_i X_j} = \frac{\nu_{X_i X_j}}{\sigma_{X_i} \sigma_{X_j}} \tag{7}$$

where the standard deviation is defined by $\sigma_{X_i} = \sqrt{\nu_{X_i}}$

The advantage of the correlation is that it is independent of the scale, i.e., changing the scale of measurement of the variables does not change the value of the correlation. Therefore, the correlation is more useful as a measure of association between two random variables than the covariance. The correlation is in absolute value always less than 1, close to zero if the random variables $X_i$ and $X_j$ are independent of each other.

An empirical estimation of these quantities require a number of observations. Suppose that $\{x_i\}_{i=1}^n$ is a set of $n$ observations of a variable vector $X$ in $\Re^p$. Each observation $x_i$ has $p$ dimensions: $x_i = (x_{i_1}, x_{i_2}, ..., x_{i_p})$, and it corresponds to an observed value of a variable vector $X \in \mathbb{R}^p$. The covariance of two random variables is then estimated as:

$$V_{X_i X_j} = \frac{1}{n-1} \left( \sum_{k=1}^{n} x_{i_k} x_{j_k} - n \overline{x}_i \cdot \overline{x}_j \right) \tag{8}$$

and the variance of a random variable is estimated as:

$$V_{X_i} = \frac{1}{n-1}\left(\sum_{k=1}^{n} x_{i_k}^2 - n\overline{x}_i^2\right) \tag{9}$$

The correlation of two random variables is then given by:

$$r_{X_iX_j} = \frac{V_{X_iX_j}}{s_{X_i}s_{X_j}} \tag{10}$$

with $s_{X_i} = \sqrt{V_{X_i}}$.

The theoretical covariances among all the random variables can be put into matrix form, i.e. the covariance matrix:

$$\Sigma = \begin{pmatrix} \nu_{X_1} & \cdots & \nu_{X_1X_p} \\ \vdots & \ddots & \vdots \\ \nu_{X_1X_p} & \cdots & \nu_{X_p} \end{pmatrix} \tag{11}$$

The estimated (empirical) version of the covariance matrix is then given by:

$$S = \begin{pmatrix} V_{X_1} & \cdots & V_{X_1X_p} \\ \vdots & \ddots & \vdots \\ V_{X_1X_p} & \cdots & V_{X_p} \end{pmatrix} \tag{12}$$

Let $X$ be a p-dimension random variable of expected value $\mu = (\mu_{i_1}, \mu_{i_2}, ..., \mu_{i_p})^T$ and covariance matrix $\Sigma$. If $X$ has a multinormal distribution, then $X$ has a probability density function (PDF) $f(x)$ defined by:

$$f(x) = \frac{1}{\sqrt{det(2\pi\Sigma)}} \cdot exp\left[-\frac{(x-\mu)^T\Sigma^{-1}(x-\mu)}{2}\right] \tag{13}$$

The probability of any subset $A \in \mathbb{R}^p$ is given by the following multiple integration formula:

$$P(A) = \frac{1}{\sqrt{det(2\pi\Sigma)}} \int_{A_1} \cdots \int_{A_p} exp\left[-\frac{(x-\mu)^T\Sigma^{-1}(x-\mu)}{2}\right] dx_1 \cdots dx_p \tag{14}$$

Thus, using the multinormal hypothesis, it is possible to estimate the actual probability density functions which must be integrated considering the actual boundaries of the random variables in order to compute the test metrics. The multinormal assumption can be validated by computing the correlation coefficients for different standard deviations in Monte Carlo simulation. We can use a Monte Carlo circuit simulation, under process deviations, to calculate the statistical parameters of the multinormal law (mean and covariance matrix) which are required.

When the number of the specifications and test criteria is important (for example, larger than 3), the number of sub-integrals in Equation (14) for the exact

computation of test metrics is too large. The computation is then impossible. To overcome this problem, as the joint PDF of performances and test criteria is assumed multinormal, a simple program implemented in Matlab (or R) is used to generate about one million instances from the multinormal distribution using a Monte Carlo technique. Next, the test metrics can be directly estimated using the following estimators:

$$\hat{Y}^D = \frac{\text{Number of functional circuits}}{N} \tag{15}$$

$$\hat{Y}_T^D = \frac{\text{Number of pass circuits}}{N} \tag{16}$$

$$\hat{Y}_L^D = \frac{\text{Number of fail functional circuits}}{\text{Number of functional circuits}} \tag{17}$$

$$\hat{D}^D = \frac{\text{Number of pass faulty circuits}}{\text{Number of pass circuits}} \tag{18}$$

where $N$ is the number of generated circuits.

We use the index $D$ to indicate that the metrics are estimated at the design stage using process deviations.

### 3.4 Test metrics computation under the presence of faults

For single parametric faults in physical parameters, test metrics can be calculated using the methodology presented by [1] where partial detectability of the parametric faults is considered. A fault is defined as the minimum value of a physical parameter $i$ that causes any performance specification to fail. This will help to calculate the probability of the occurrence $p_i^{spec}$ of this fault, which represents the probability that the value of this physical parameter is greater than $v_i^{spec}$ (Figure 6).

We calculate also the probability $p_i^{test}$ to detect a fault in this parameter, which represents the probability of this parameter to be greater than $v_i^{test}$, where $v_i^{test}$ is the minimum value of the process parameter that causes the test criteria to fail (Figure 6).

Considering theses definitions, we can write the analogue test metrics, based on the probabilities $p_i^{spec}$ and $p_i^{test}$ as follows [1]:

$$Y^F = \prod_{i=1}^{n}(1 - p_i^{spec}) \tag{19}$$

$$Y_T^F = \prod_{j=1}^{m}(1 - p_j^{test}) \tag{20}$$

$$Y_C^F = \frac{G_P^F}{Y^F} = 1 - Y_L^F \tag{21}$$

$$D^F = 1 - \frac{G_P^F}{Y_T^F} \tag{22}$$

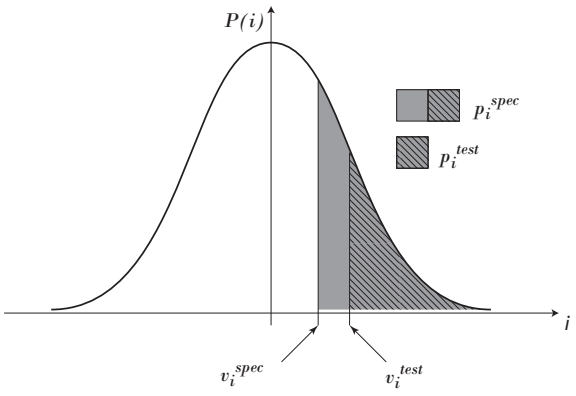



**Fig. 6.** Distribution of a parameter $i$ with associated probabilities.

where, $G_P^F = \prod_{i=1}^{n}(1 - \max(p_i^{spec}, p_i^{test}))$, which represents the probability that a circuit is functional and passes the test.

The fault coverage $F$ for the parametric faults is calculated using the following equation [1]:

$$F^F = \frac{\sum_{i=1}^{n} \ln(1 - \min(p_i^{spec}, p_i^{test}))}{\sum_{i=1}^{n} \ln(1 - p_i^{spec})} \tag{23}$$

We use the index $F$ to indicate that the metrics are calculated under the presence of faults.

## 4 Test vehicle

### 4.1 Description of the circuit

The test vehicle is a fully-differential operational amplifier. This amplifier has been designed in a $0.18\mu m$ CMOS technology from ST Microelectronics. The amplifier is formed of four main blocks: a bias circuit, a start-up circuit, a common-mode control circuit and a differential amplifier circuit. Figure 7 illustrates this circuit.

First, we use the statistical analysis to calculate the test limits for the test criteria under process deviations by calculating the analogue test metrics, in particular the defect level and the yield loss at the design stage. Then, taking into account these test limits, we calculate the fault coverage in order to test the capability of the test technique for fault detection considering both catastrophic and parametric faults. Finally, we will find the minimal set of specifications and test criteria which give the best fault coverage.

In order to find the different fitted Gaussian distributions of each circuit performance and test criteria we performed a Monte Carlo circuit simulation (1000 iterations). The comprehensive set of performances and test criteria considered is given in Tables 1 and 2, where $a_1$ and $a_2$ represent the specifications, that

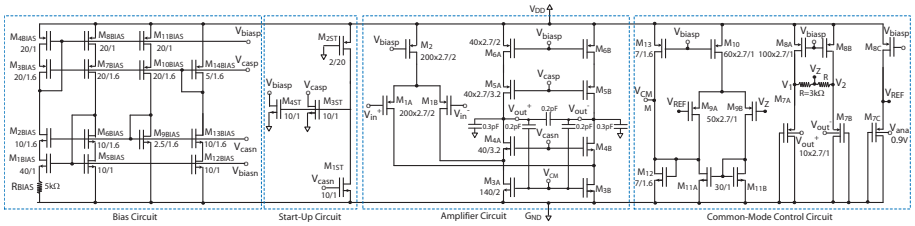



**Fig. 7.** Folded cascode fully differential amplifier. The dimensions of each transistor W/L are expressed in multiples of the unity size transistor ($W_{UNIT} = 0.28\mu m$ and $L_{UNIT} = 0.18\mu m$).

| Performance | Test bench | $\mu$ | $\sigma$ | Specification $a_1$ | Specification $a_2$ |
|---|---|---|---|---|---|
| $A_D$ | | 76.60dB | 0.493dB | 74.49dB | 78.71dB |
| $GBW_D$ | 1 | 330MHz | 18.14MHz | 252.36MHz | 407.64MHz |
| $Phase\ Margin\ \phi_D$ | | 63.33° | 0.45° | 61.40° | 65.26° |
| $CMRR$ | 2 | −42.76dB | 1.02dB | −47.13dB | −38.39dB |
| $PSRR\ (G_{ND})$ | 3 | −29.99dB | 3.65dB | −45.61dB | −14.37dB |
| $PSRR\ (V_{DD})$ | 4 | −28.21dB | 3.75dB | −44.26dB | −12.16dB |
| $THD$ | 5 | 66.19dB | 2.38dB | 56.00dB | 76.38dB |
| $Current\ (I_{DD})$ | | 2.48mA | 0.21mA | 1.58mA | 3.38mA |
| $Intermodulation$ | 6 | 67.57dB | 1.09dB | 62.90dB | 72.24dB |
| $SR+\ (C_L = 1pF)$ | 7 | 73.14V/$\mu$s | 5.55V/$\mu$s | 49.38V/$\mu$s | 96.88V/$\mu$s |
| $SR-\ (C_L = 1pF)$ | | 73.14V/$\mu$s | 5.55V/$\mu$s | 49.38V/$\mu$s | 96.88V/$\mu$s |
| $In\ Ref.\ Noise$ $(BW = 20kHz)$ | 8 | 39.22$\mu$V | 0.5$\mu$V | 37.08$\mu$V | 41.36$\mu$V |

**Table 1.** The performances of the amplifier with their Gaussian parameters and the specifications set at $4.3\sigma$.

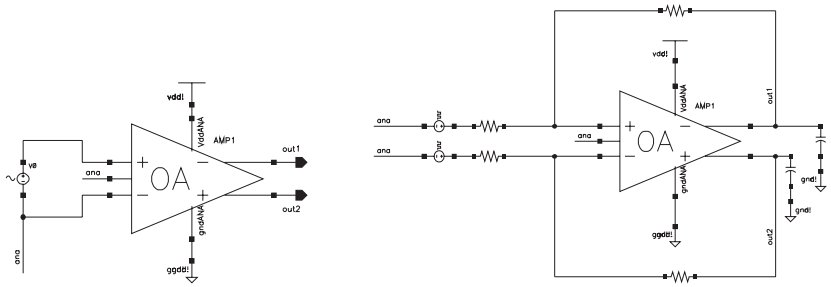
is, the bounds of each performance. The specifications of the amplifier are not known a priori, since the actual system application of the device is not considered in this work. Thus, we have set ourselves the specification bounds in order to have a high yield at the design stage of $Y^D = 99.99\%$ when all performances are considered. This requires a tolerance interval of $\mu \pm 4.3\sigma$ for each performance. The test limits $b_1$ and $b_2$ will be calculated by the technique which will be presented below.

Different test benches have been used to calculate the different performances. For example, Figures 8(a) and (b) show the test benches n° 1 and n° 7, respectively. Each test bench allows the calculation of one or more performances and test criteria. Table 1 shows the specifications with the actual test bench used for the calculation. Eight different test benches are required for the performances.

For the actual test of the fully differential amplifier, the measurement of the $SNDR$ of the amplifier is considered using a sine-wave fitting technique

| Test criteria | Test bench | $\mu$ | $\sigma$ | Test limits | |
|---|---|---|---|---|---|
| | | | | $b_1$ | $b_2$ |
| SNDR | 9 | 68.85 dB | 2.19 dB | To determine | To determine |
| Offset | | 0 $\mu V$ | 7.69 $\mu V$ | To determine | To determine |

**Table 2.** The test criteria of the amplifier with their Gaussian parameters.




(a) (b)

**Fig. 8.** Example of the test bench n°1(a) and n°7(b) of the amplifier.

described in [11, 17]. The DC Offset of the amplifier is also considered as a possible test criteria that can be measured using the sine-wave fitting technique. To simulate these test measurements, an additional test bench is required.

The total Monte Carlo circuit simulation time of 1000 instances, considering the 8 test benches for the performances and the $9^{th}$ test bench for the test criteria, is 3 hours. The overall process is fully automated using the CAT platform.

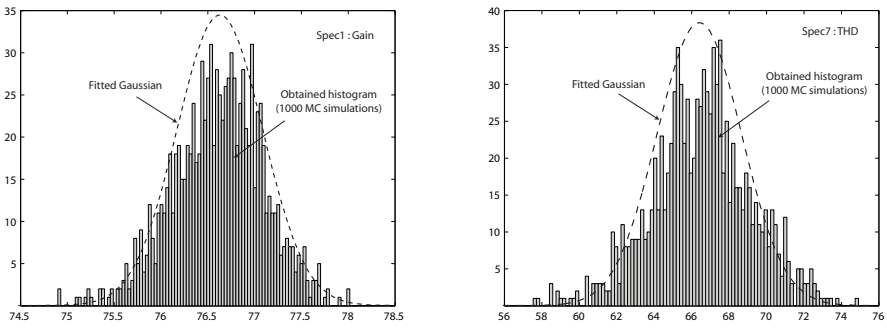
As we can see in Figures 9(a) and 9(b), the distributions of the *Gain* and the $THD$ are very close to the multinormal one. The same results are obtained for the other performances and test criteria.

### 4.2 Precision on test metrics estimation

We need to find the test limits to separate the faulty circuits from the fault-free ones, as a function of the required test metrics. A trade-off between Defect level and Yield loss must be considered under process deviations, and this will set the actual test limit.

Using the equations (1) to (4) presented in Section 3.2 these test metrics at the design stage can be theoretically calculated. However, in our case, we have 12 specifications, and it is not feasible to perform the integration with such a large number of integrals. Thus, we will use the Monte Carlo method of estimation proposed in Section 3.3.

In order to see the accuracy of this method, we will first illustrate a simpler case when only two performances, $Phase\ Margin$ and $THD$, are considered together with the test criterion $SNDR$. In this case, the metrics presented by




(a) (b)

**Fig. 9.** The distribution of the *Gain* $A_D$ (a) and the $THD$ (b) of the amplifier.

(1) to (4) are calculated as follows:

$$Y^D = \int_{A_3} \int_{A_7} f(s_1, s_2)\ ds_1\ ds_2 \tag{24}$$

$$Y_T^D = \int_{B_1} f(t_1)\ dt_1 \tag{25}$$

$$Y_L^D = 1 - \frac{G_P}{Y} \tag{26}$$

$$D^D = 1 - \frac{G_P}{Y_T} \tag{27}$$

where

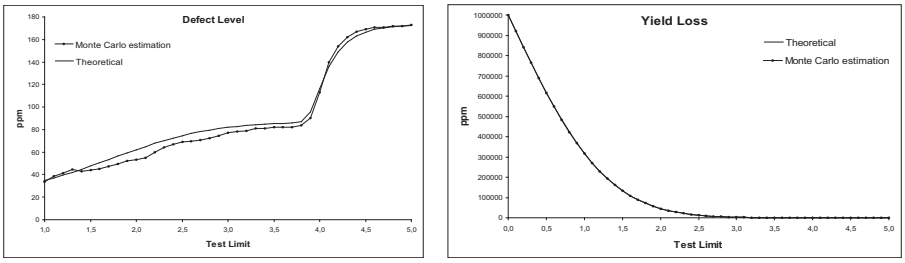
$$G_P^D = \int_{A_3} \int_{A_7} \int_{B_1} f(s_1, s_2, t_1)\ ds_1\ ds_2\ dt_1$$

is the probability that the circuit is functional and passes the test, $s_1$ is the *Phase Margin* value, $s_2$ is the $THD$ value, $t_1$ is the $SNDR$ value, $A_i$ is the $i^{th}$ specification, $B_1$ is the test limit of the $SNDR$ and $f(.)$ is calculated by (13). The covariance matrix $\Sigma$ is estimated by $S$ given by (12).

For a given test limit, these metrics can be calculated exactly in this case, because the number of integrals is small.

Figure 10(a,b) shows that the estimated (Monte Carlo algorithm) and the theoretical values of the metrics are very close for the case of Defect level and Yield loss.

For comparison, Figure 11(a) shows the distributions of the *Phase Margin* and the $SNDR$ for the case of 1000 instances obtained via Monte Carlo circuit simulation and for the case of 1000 instances generated from the multinormal distribution with a Monte Carlo technique. From this Figure, it is clear that both distributions are the same. The same results have been obtained for the other performances and test criteria. In addition, Figure 11(b) shows the generation of




(a) (b)

**Fig. 10.** Comparison of the estimated and the theoretical test metrics for the case of two specifications and one test criterion: (a) Defect level and (b) Yield loss.

1000 and 1 million circuit instances generated from the multinormal distribution. It is clear that with 1 million instances we will reach the required ppm precision.

### 4.3 Test limit setting under process deviations

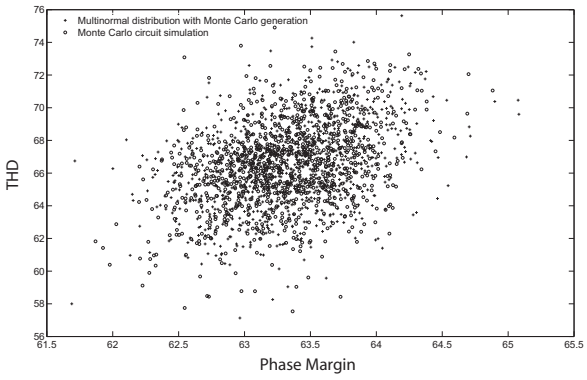
The setting of test limits is always a trade-off between test cost and test quality. Here, just as an example for our case-study, we will consider setting the test limits that simultaneously try to minimise both Defect Level and Yield Loss. Figure 12(a) shows Defect Level and Yield Loss together as a function of the test limits of $SNDR$ and $I_{DD}$, where the intersection between them is of interest to us.

We have introduced here as test criterion the current consumption $I_{DD}$, since we will se it is important fault detection. The test limits for $I_{DD}$ is given by $(\mu_{IDD} \pm k_{IDD}\ \sigma_{IDD})$.

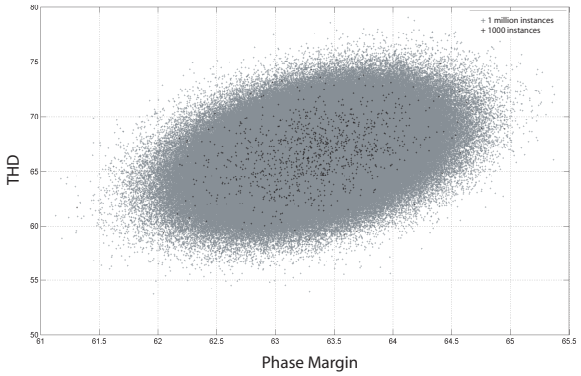
This intersection (points where the Defect Level is equal to the Yield Loss) is redrawn in Figure 12(b). We have chosen as trade-off of the test limits of the $SNDR$ and the $I_{DD}$ the minimum of these points which is equal to $55ppm$. This results in a test limit of $4.0\sigma$ for the $SNDR$ and $4.1\sigma$ for the $I_{DD}$.

### 4.4 Fault coverage under the presence of catastrophic faults

We have considered catastrophic faults that result in shorts and opens in all the transistors, resistances and capacitances of the amplifier. This results in 160 catastrophic faults. Figure 13 shows the fault coverage given by the measurement of each performance and several possible test criteria with the test limits fixed as explained before. The performances allow to detect 98.12% of faults where the undetected faults occur in the Bias block. On the other hand, the test criterion $SNDR$ allows the detection of 89.38% of the faults. The undetected faults occur also in the Bias block. Maximum fault coverage can be achieved if power consumption $(I_{DD})$ is considered in addition to the $SNDR$ measurement.




(a)



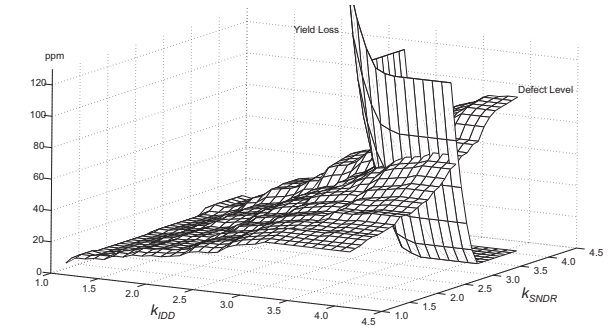

(b)

**Fig. 11.** (a) Distribution of 1000 circuits generated by Monte Carlo circuit simulation and from the multinormal law and (b) generation of 1000 and 1 million circuits from the multinormal distribution.

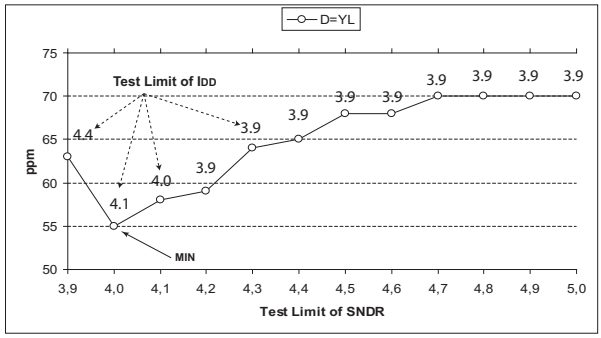
### 4.5 Test metrics under the presence of parametric faults

We consider parametric faults as a result of a physical parameter deviating beyond an acceptable value. The physical parameters considered include the L and W of the PMOS and NMOS transistors and the resistance and capacitance values. We note that L and W of the transistors are not process parameters, and thus their deviations are not included under process deviations. On the other hand, resistance and capacitance values deviate under process deviations.

In order to calculate the probabilities $p_i^{spec}$ and $p_i^{test}$ for each potentially faulty physical parameter, we have to obtain by simulation its limit deviation values. The distribution of each physical parameter is considered as Gaussian with mean equal to the typical value of this parameter. A standard deviation of $10nm$ is taken for L and W of the transistors and 5% for the resistances and the




(a)




(b)

**Fig. 12.** (a) The Defect Level and the Yield Loss as a function of the $SNDR$ and $I_{DD}$ test limits, (b) The test limits of the $SNDR$ and the $I_{DD}$ where the Defect Level and the Yield Loss are equal.

capacitances. Thus, for each varying physical parameter, we have injected in the amplifier deviations from -20% to 100%. For each value of a physical parameter, all test benches must be simulated. A dichotomic search is applied to find the limit deviation for each physical parameter.

This process has resulted in the consideration of 180 potentially faulty physical parameters, where only 13 of them result in a specification violation. These faults are listed in Table 3 together with their probabilities. The other faults have a negligible probability of occurrence ($p_i^{spec} = 0$). We note here that deviations in transistors that are matched cannot be considered individually. They are considered by injecting the same deviation in all matched transistors. We have seen that faults in all matched transistors have a negligible probability. In order to consider the faulty behaviour resulting from mismatch, it is necessary to use the mismatch option in the Monte Carlo circuit simulation. In this work, we have used the process option for this, but a similar analysis could be performed for mismatch deviations.

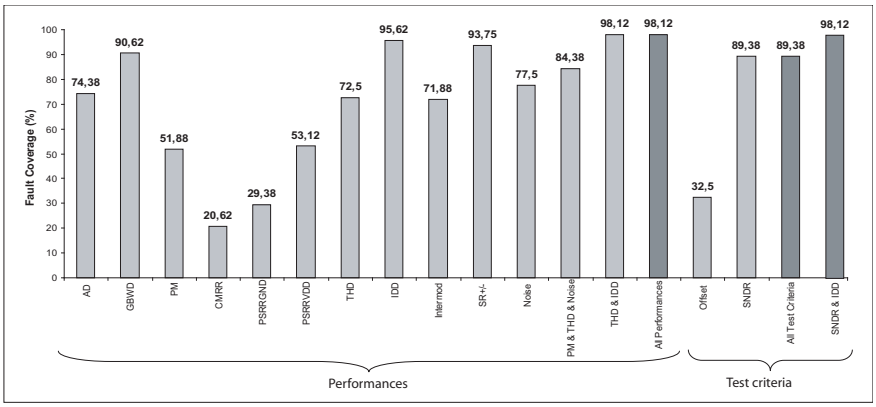



**Fig. 13.** Catastrophic fault coverage of the different specifications and several possible test criteria.

Using these parameters and Equations (19) to (23), the values of the different test metrics are given in Table 4. We consider two cases: in the first case, all 13 parametric faults are considered. Only 2 of these faults are not detected by the test criteria (SNDR, Offset and Current Consumption), this is why the fault coverage does not reach 100%. The fault coverage $F^F$ is high because the undetected faults have lower probability. Notice that the yield $Y^F$ is lower than 60%, much lower than the design yield $Y^D$ that has a value above 99%. This is because deviations of physical parameters such as L and W are not considered under process deviations. The second case of Table 4 does not consider deviations in the physical parameters L and W, but only in the resistance values (faults due to capacitance deviations have negligible probabilities). In this case, fault coverage $F^F$ reaches 100% with a yield $Y^F$ above 99%. Since these deviations are also considered as process deviations, we obtain similar results between $Y^F$ and $Y^D$.

## 5 Conclusions and Future Work

This paper has introduced a CAT platform for analogue and mixed-signal test evaluation. In particular, fault simulation and test optimization are considered. Catastrophic faults can be tackled in a similar way as for digital circuits, regardless of the circuit specifications, although process deviations may need to be considered. Single parametric faults have been considered (based on the approach of [1]). A statistical approach for the estimation of test metrics and the setting of test limits under process deviations is the major contribution of this paper. The data for this approach is obtained from a Monte Carlo simulation. Test optimization for a fully differential amplifier has been illustrated as a case-study.

| No | Component (Parameter) | Fault | $p^{spec}$ | $p^{test}$ |
|---|---|---|---|---|
| 1 | MP1 (l) | +12.21% | 0.013996 | 0.013996 |
| 2 | MP3 (l) | +7.32% | 0.093690 | 0.093690 |
| 3 | MP5 (l) | +22.95% | 0.000009 | 0.000009 |
| 4 | MP1 (l) | −3.18% | 0.283305 | 0.283305 |
| 5 | MP3 (l) | −11.70% | 0.017604 | 0 |
| 6 | MP18 (l) | −15.76% | 0.002270 | 0 |
| 7 | MN2 (l) | −16.23% | 0.001736 | 0.001736 |
| 8 | MN4 (l) | −6.46% | 0.122278 | 0.122278 |
| 9 | R1 (r) | +15.14% | 0.001227 | 0.001227 |
| 10 | R4 (r) | +17.09% | 0.000308 | 0.000308 |
| 11 | R7 (r) | +16.11% | 0.000628 | 0.000628 |
| 12 | R4 (r) | −12.79% | 0.005249 | 0.005249 |
| 13 | R7 (r) | −16.15% | 0.000611 | 0.000611 |

**Table 3.** Parameters used to calculate the metrics for the case of parametric faults.

| Metric | All parametric faults | Resistor faults only |
|---|---|---|
| $F^F$ | 96.69% | 100% |
| $Y^F$ | 54.56% | 99.22% |
| $Y_T^F$ | 55.56% | 99.22% |
| $Y_C^F$ | 100% | 100% |
| $D^F$ | 1.98% | 0% |

**Table 4.** Test metrics values for single parametric faults.

## Acknowledgements

The authors would like to acknowledge the fruitful discussions on analogue parametric testing with Jean Louis Carbonéro, ST Microelectronics, France.

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