Photonic Firewall Oriented Fast All-Optical Binary Pattern Recognition

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***Abstract*—We propose an all-optical logic gate based binary sequence matching system for OOK modulated format optical signals at high information rate by using cross-phase modulation (XPM) and four-wave mixing (FWM) in high nonlinear fiber (HNLF). Through the simulation successfully demonstrates that the system can identify and locate the known 8bit detection sequence from the input 64bit target sequence at the information rate of 80Gbps.**

Keywords—sequence matching, high nonlinear fiber, All optical logic gate, cross-phase modulation, four-wave mixing

I. Introduction

With the rapid development of information technology, optical network technology also needs to usher in a great innovation. The construction of ordinary optical network is often inseparable from the support of electrical nodes, it is the presence of these electrical nodes that makes the transmission speed and transmission quality of signals are greatly limited by frequent optical/electrical and electrical/ optical conversions carried out in optical network. All-optical networks replace electrical nodes in the network with optical nodes, so that the optical signal in the network can rarely carry on the transmission and processing in the optical domain, so as to improve the signal transmission speed and transmission capacity. Like normal networks, all-optical networks are subject to a variety of attacks, such as traffic analysis, eavesdropping, signal delay denial of service, etc. Although there are many kinds of attack ways, they all have some common characteristics. The most obvious feature is that non-authenticated users attacking optical networks always use the same IP address, or attackers always carry out persistent attacks on a fixed port number in optical networks. According to this feature, firewall can be used to identify the input optical network signal, identify whether the signal contains specific source address and destination address, and then determine whether the signal is a malicious attack signal.

In all - optical network, we need to use photon firewall instead of ordinary electronic firewall. Binary sequence matching system is the main component of photon firewall.in [1], the European wisdom (wire-speed security domain with light monitoring) project is dedicated to the development of a photon firewall for the detection and monitoring of optical domain signals. In [2-3], Cotter et al. designed the matching of a single all-optical logic AND gate binary sequence which can match a fixed target sequence. And in [4], a matching system built by XNOR gate, AND gate and regenerator designed from semiconductor optical amplifier - based Mach - Zehnder interferometer (SOA - MZI) was proposed, which can rarely match OOK format target sequence at 42Gbps because of the long carrier recovery time of SOA.

As a special passive optical device, HNLF (high nonlinear fiber) has extremely high nonlinear coefficient and high response speed, and has become an excellent device that can replace SOA to realize all-optical logic gate.

In the paper we propose a binary sequence matching system for OOK signals based on logic gates and wavelength conversion by using four-wave mixing (FWM) and cross-phase modulation (XPM) in HNLF.

II. Concept

Logic gate is the most important part of binary sequence matching system. Its function is to process the input signal according to certain logical relation and then output the result of logical operation. In[4], the binary matching sequence is mainly composed of XNOR logic gate AND logic gate, shown in Fig. 1.And the truth table of common logical operations is shown in Table I.

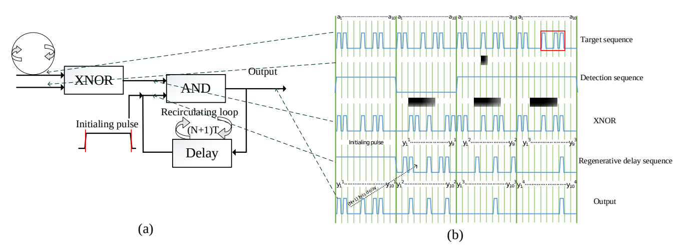

Fig. 1 Binary sequence mathing system: (a) Schematic diagram (b) Output diagram of each module

Fig. 1.(a) is the schematic diagram of this system, where M is the length of the detection sequence, T is the symbol time width, and N is the length of the target sequence. Extending each bit of the detection sequence to N bits can produces an input of length $N \cdot M$. Then the target sequence is cycled M times to generate a sequence of length $N \cdot M$. The final system will match the detection sequence in the target sequence and the output signal is γ. As shown in Fig. 1.(b), matching the 4bit detection sequence requires the system to cycle for 4 times and

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TABLE. I TRUTH TABLE OF COMMON LOGICAL OPERATIONS

Input signals A B	Output of logic operations					
	AND($A\cdot B$)	*XOR*($A\oplus B$)	*NXOR*($A\odot B$)	*NOT*($\overline{A}$)	*Left-XOR*($\overline{A}B$)	*Right-XOR*($A\overline{B}$)
0 0	0	0	1	1	0	0
1 0	0	1	0	0	0	1
0 1	0	1	0	1	1	0
1 1	1	0	1	0	0	0

the system will output a pulse in the last position of the detection sequence in the target sequence.

Base on Table I, XOR and XNOR are a pair of opposite logical operations, and we can get the following relationship:

$$A\oplus\overline{B} = A\overline{\overline{B}} + \overline{A}\,\overline{B} = AB + \overline{A}\,\overline{B} = A\odot B \qquad (1)$$

Base on (1), after replacing the XNOR logic gate of the above system with the XOR logic gate, the NOT logic of the sequence can be input to keep the correctness of the sequence matching.

The spectrum of the probe light with lower signal input power generates a frequency offset induced by XPM effect under the influence of pump light with higher signal input power in HNLF, and in [5], the AND logic gate and the XOR logic gate can be realized with the help of XPM in HNLF. The XOR logic gate realized by coupling the output light of two logic gates: $A\overline{B}$ and $\overline{A}B$, but the wavelength of this two beams is different. In order to make the output light of XOR logic gate at the same wavelength, we convert the wavelength of $\overline{A}B$ through FWM effect in HNLF, so that the two lights at the input of the coupler only have one wavelength.

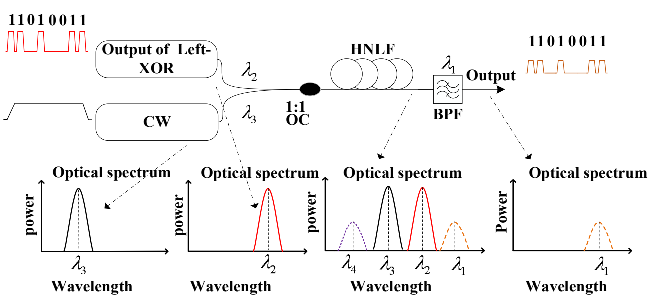

Fig. 2 Wavelength conversion based on FWM effect

The wavelength conversion through FWM effect in HNLF is shown in Fig. 2.

When two or more lights of different wavelengths satisfying phase matching are injected into the nonlinear medium(such as HNLF), FWM effect will occur between the lights, and two new frequency components will be generated. The relation of four wavelengths in Fig. 2 is:

$$\begin{cases} \lambda_3 = 2\lambda_2 - \lambda_1 \\ \lambda_1 = 2\lambda_2 - \lambda_3 \\ \lambda_4 = 2\lambda_3 - \lambda_2 = 3\lambda_2 - 2\lambda_1 \end{cases} \qquad (2)$$

Base on (2), we can realize the wavelength conversion by design the wavelength λ_3 of continuous wave(CW).

III. System Setup

The binary sequence matching system based on the nonlinear effects in HNLF is tested by using VPI simulation software. The optical logic gate and wavelength conversion module can cause the strength loss of the input optical signal, so the output signal of each part is amplified by using the ideal EDFA. The sequence pattern matching system for OOK signal based on nonlinear effect in HNLF proposed in this paper is shown in Fig. 3.

The flow of the first cycle of the binary sequence matching system is shown in Fig. 3,the input target sequence is 11010011, In order to match the sequence that first bit is 1 in the target sequence, the detection sequence needs to input 00000000. Then, input the XOR logic output of 11010011 into AND logic gate. The other input of AND logic gate should be the delay signal of its output signal, so an initial pulse 11111111 should be input into the AND logic gate in the first cycle, and then the output signal of the first cycle should be used as the input signal of the second cycle after the delay. In the first cycle, the output of the binary sequence matching system is 11010011, so the number and position are obtained.

The system consists of two parts: the XOR logic gate and the AND logic gate. In the XOR logic gate section, the optical signal of the target sequence and the optical signal of the detection sequence are divided into two beams by two 1:1 optical couplers(OC) respectively. The wavelength of system input target sequence is λ_1=1570.68 nm, the peak power is $P_1 = 300mW$. And the wavelength of probe light is λ_2=1550.227 nm, the peak power is $P_2 = 300mW$.The resulting beams are then transmitted to HNLF1 and HNLF2 through OC3(1:9) and OC4(9:1), respectively. In the Left-XOR logic gate, the detection sequence signal is probe light and the target light is pump light. In the Right-XOR logic gate, the detection sequence signal is pump light and the target light is probe light. The length of HNLF1 is $L_1 = 200m$, the nonlinear index is $N_1 = 50\times10^{-20} m^2/W$, the zero dispersion wavelength is $\lambda_a = 1570.68nm$, and the dispersion slope is $s_1 = 0.08\times10^3 s/m^3$. The specification parameters of HNLF1 and HNLF2 used in this system to realize XPM effect are exactly the same. The gain of EDFA1 is same as the gain of EDFA2,which is12.55dB. The central wavelength of BPF1 is λ_2 and The central wavelength of BPF2 is λ_1. The wavelength conversion part converts the

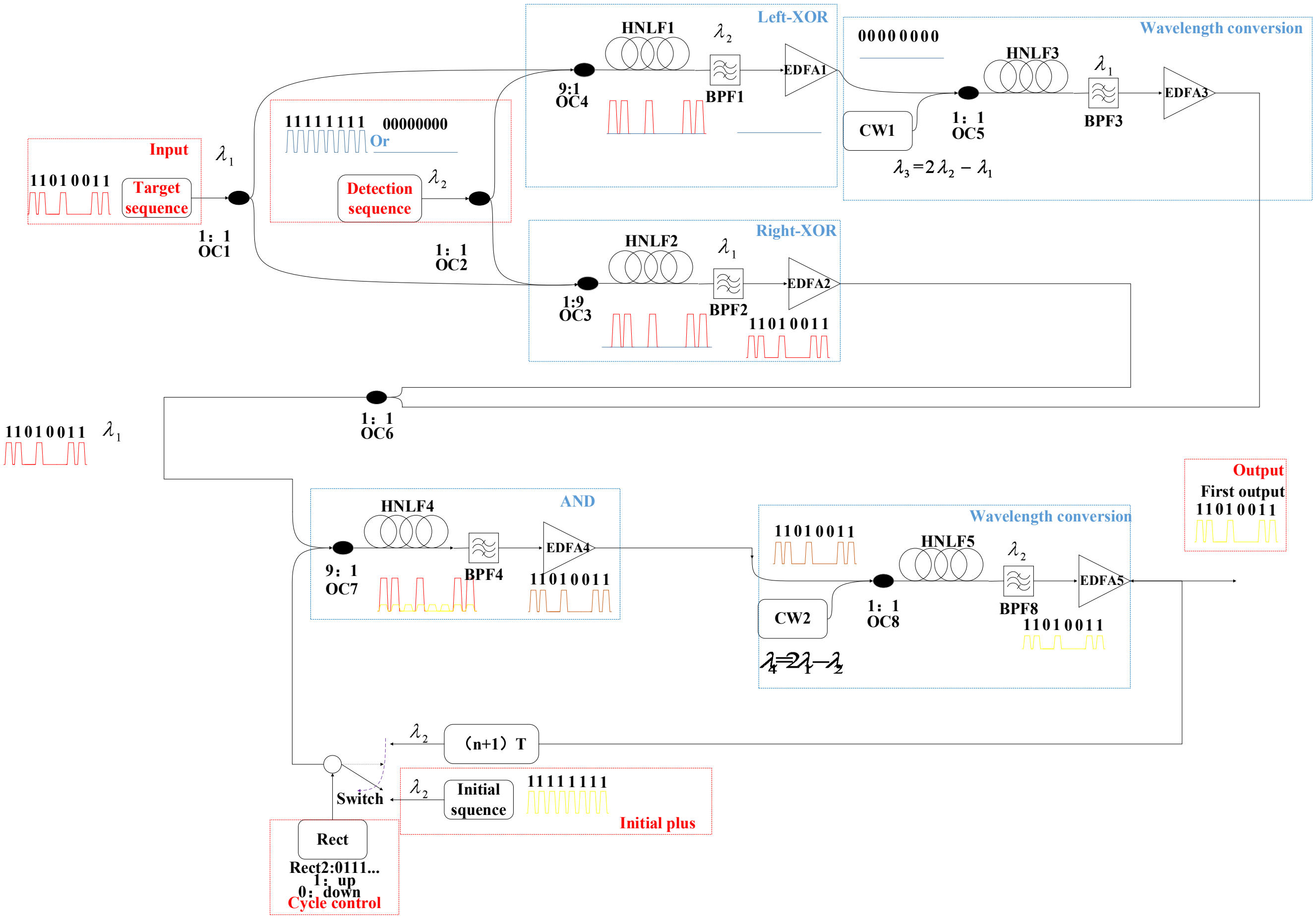

Fig. 3 Binary signal sequence pattern matching system

wavelength λ_2 of output light in Left-XOR logic gate to λ_1. CW1 has a wavelength of $\lambda_3 = 1530.3nm$ and a peak power of $P_3 = 100mW$. The length of HNLF3 is $L_1 = 20m$, the nonlinear index is $N_1 = 21\times10^{-20} m^2/W$, the zero dispersion wavelength is $\lambda_b = 1550.2nm$, and the dispersion slope is $s_3 = 0.08\times10^3 s/m^3$. The central wavelength of BPF3 is λ_1. The gain of EDFA3 is $51.37dB$.

The above two processed lights are coupled through OC6 (1:1) to obtain the XOR logical output. In AND logic gate, the specification parameters of HNLF4 are the same as the parameters of HNLF1 and HNLF2. The output light of XOR logic gate is the probe light and the initial pulse is the pump light, and they are coupled to HNLF4 by OC7 (1:9). The gain of EDFA4 is 15.55 *dB,* the central wavelength of BPF4 is λ_5=1560.3 *nm*.

The output signal of the AND logic gate needs to undergo wavelength conversion and signal amplification before delay. The gain of EDFA4 is12.55*dB*.The specification parameters of CW2 and HNLF5 are the same as the parameters of CW1 and HNLF3. The central wavelength of BPF4 is λ_2, and the gain of EDFA5 is 51.37*dB*.

The output signal of the system will be input into AND logic gate again after delay processing, and the delay time is $t = (n+1)\times T$. T is the time interval of each bit of data of the input signal and is inversely proportional to the bit rate of the input signal, while n is the length of the input target sequence. The input signal rate adopted by this system is 80Gbps.

IV. Results and Discussion

In Fig. 4, we show that when the input target sequence length is 64bit and the rate is 80Gbps, the output of the binary sequence matching system each cycle, and the length of detection sequence is 8bit.

At the rates of 80G bit/s, the 8bit detection sequences is 01101101. In Fig. 4, the location of the detection sequence in the target sequence is marked and (a-b) correspond to the output of the system in each cycle. In the first cycle, the actual target sequence is 0, but the target sequence set by the system is 1. The system will firstly output the position of the sequence which the first bit is 0 in the target sequence. And (a) indicates the position of these sequences. Similarly, (b) represents the position of the sequence with the first two bits are "0" and "1" in the target sequence. After eight cycles, we can get the number and position of the detection sequence 01101101 in target sequence, shown in (h) of Fig. 4.

At present, the system has restriction on the format of input signals. When it is necessary to sequence match signals of other modulation formats, the signal needs to be converted into OOK signal through format conversion.

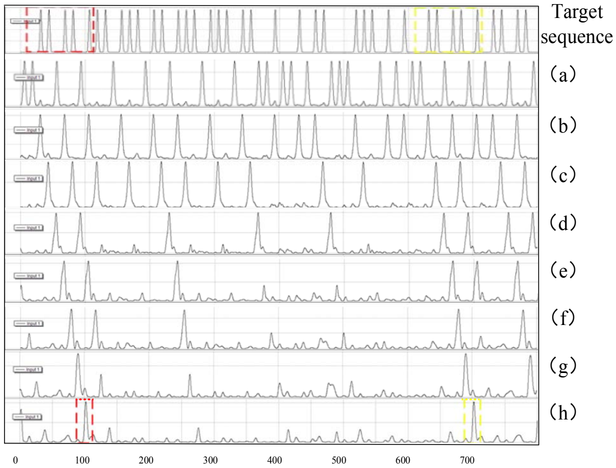

Fig. 4 Eye diagram of 8bit detection sequence matching output under 80G bit/s

In addition, the XOR logic gate and the AND logic gate are realized base on the spectrum offset effect of XPM. However, in the case of large signal rate, the frequency offset of XPM is insufficient. In this way, it is inevitable that there is some residual power in the output signals of logic gate at the position where the signal strength should be 0 in theory. The residual power continues to be input into the AND logic gate as part of the output signal during each cycle. With the continuous increase of the number of cycles, the residual power is continuously accumulated. When the residual power reaches a certain value, the system will misjudge the signal. This is why at present the system can only match 8bit detection sequence at 80Gbit rate. The problem of residual power can be generally solved by means of waveform shaping. Therefore, we will focus on the implementation of all-optical regenerator at high bit rate.

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