Some Hardware Aspects of the BESM-6 Design

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Abstract. This paper very shortly describes some hardware solutions of central processor (CPU) of BESM-6. CPU had very deep instruction pipe with an associative buffer for instructions and an associative buffer for data with original protocol. Logical and storage elements used only domestic discrete components. Main logical unit based on differential amplifier with pyramid of rich diode logic and paraphase synchronization. Original construction without printed plate made wire connections very short and gave possibilities for direct access to every contacts and interchanging modules. All these solutions permitted to achieve high clock frequency, reliability and effective maintenance.

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Keywords: General-purpose computer architecture, instruction pipe, logic circuit design, mechanical package

1 Introduction

The Institute of Precise Mechanics and Computer Engineering (IPMCE) developed the general-purpose computer BESM-6 under the leadership of academician S.A. Lebedev. It became operational in 1967. The BESM-6 integrated the latest architecture features and domestic experiences with many original solutions that provided high efficiency and exclusively a long period of exploitation.

First computers were installed in major scientific and cosmic institutions and had played important role in research and development domestic science, defense and technology. Later BESM-6 had undergone several modifications and successfully operated in different fields of industry and education as one of the most popular general-purpose computer. Up to four hundred computers were produced with modifications of input/output and memory parts and some computers are known in working state nowadays.

This paper is devoted to some hardware aspects of the BESM-6 central processing unit piping not reflected in other paper about software.

2 BESM-6 Characteristics

Figure 1 shows the front view of the BESM-6 CPU in its working state in 2006. Some of its general characteristics include the following:

- 48-bit word with 2 parity bits in memory (one for each half-word)

- Two 24-bit single-address instructions with two formats in one program word
- General-purpose operation set with floating-point arithmetic
- 15-bit address space with extension possibilities
- Wide set address transformations with stack mode included
- Page mode protect system for memory
- Privilege mode program execution
- Extended concurrent i/o operations
- Hardware support for interrupts
- Efficiency and exclusive reliability, with other features

Fig. 1. Front view of the BESM-6 central processing unit.

Of particular importance in achieving high performance was flexible instruction pipeline for the CPU with large throughput and deep look ahead. Its integration with all previously mentioned characteristics permitted to create large amount of mathematical software and application packages. During the BESM-6 lifecycle, rich software was designed including compilers for all known programming languages, operating systems, and application packages as the largest domestic soft fund.

3 Basic Architecture

BESM-6 pipeline was designed independently of well-known Stretch computer; its chief designer S.A. Lebedev called it a “water pipeline”. It was investigated in detail

on a program model. The pipeline architecture of the BESM-6 CPU actually had all features of contemporary microprocessors but with very limited resources.

Original logic elements with paraphase synchronization allowed creating flexible command pipeline for the CPU with 300 ns instruction cycle time and deep look ahead (six and more instructions). Unique torodial ALU with very fast cycle time. The general block-diagram of BESM-6 central processing unit appears in Fig. 2.

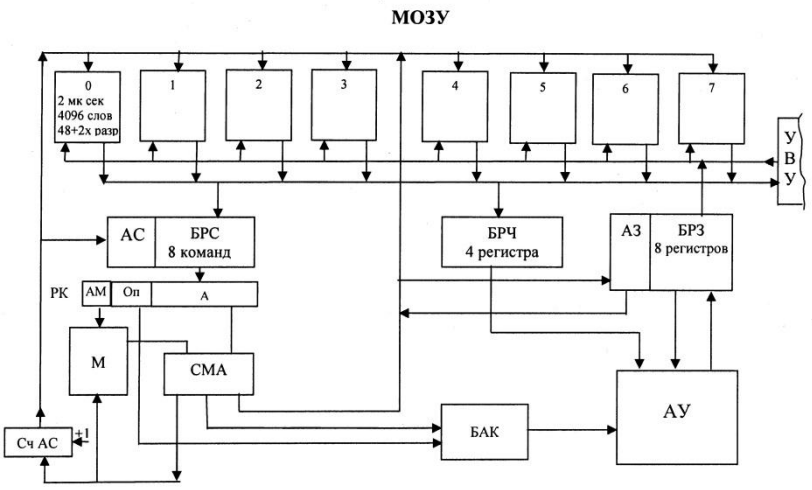

Fig.2. General block-diagram of BESM-6 central processing unit.

Main functional units:

МОЗУ	–	magnetic ring storage with blocks of 4096 (48+2 bit) words with 2 microseconds cycle time.
АС-БРС	–	associative buffer (8 instructions) with 300 ns cycle time.
РК (АМ, Оп, А)	–	instruction register, where: АМ – address of index registers (М), Оп – operation code, and А – operand address.
СМА	–	adder for address modification.
БАК	–	buffer for arithmetic commands.
БРЧ	–	buffer for operands from memory (300 ns).
АЗ-БРЗ	–	associative buffer for results written to the main memory (300 ns). The oldest unused result was transferred to memory.
АУ	–	toroidal multifunctional ALU with many interesting solutions for special paper.

The control unit coordinates control the operation of all functional units and it includes an interrupt system, I/O operation, and many other functional units to support effective work of operating system.

The base for the system of semiconductor logical elements was a differential amplifier with common emitter and wide pyramid of diode logic (Fig. 3). It included back link gates for the latch function and had an AND-OR-AND-pyramid to set the latch in definite state. One may say that this logical element base supported original construction solutions that allow the design of a very effective and reliable computer.

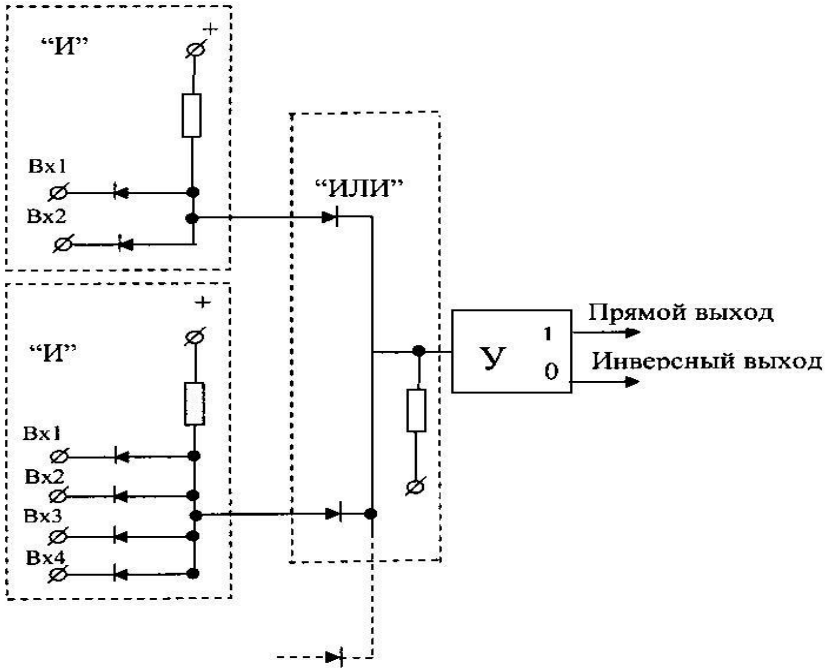

Fig. 3. Basic logical unit

Four amplifiers with backward gates were placed in one physical block (Fig. 4) with their state indicators. Input logic was in other physical block (Fig. 5), which was placed on the opposite side of chassis as close as possible to keep wires short (Fig. 6). It is the use of all these constructive solutions with an original paraphase synchronization based on two sinusoidal signals with 10 MHz frequency that permitted a clock of 100 ns in pipeline processing.

The integral use of all mentioned solutions allowed them to reach a rate of 1 MIPS using ordinary domestic semiconductor technology, which had the best components per operation ratio.

Four chasses with У-blocks were placed in one cabinet and four adjoining cabinets, showed in Fig. 1, display all CPU latches and permit direct physical access to all contact points for oscillograph.

The test and diagnostic system provided extremely high results in maintenance and finding accidental faults. All this made possible extremely long periods of reliable operation in many computing centers.

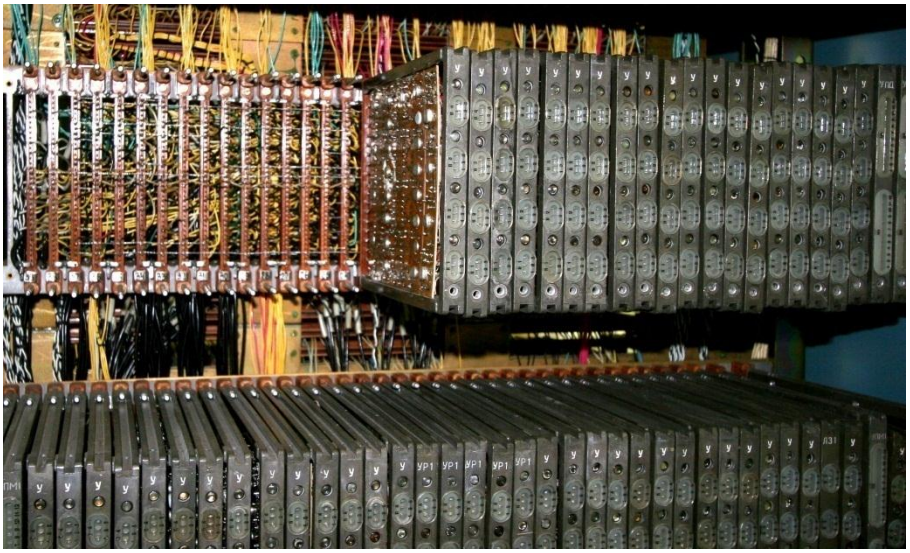

Fig. 4. Fragment of chassis with У blocks

Fig. 5. Д block.

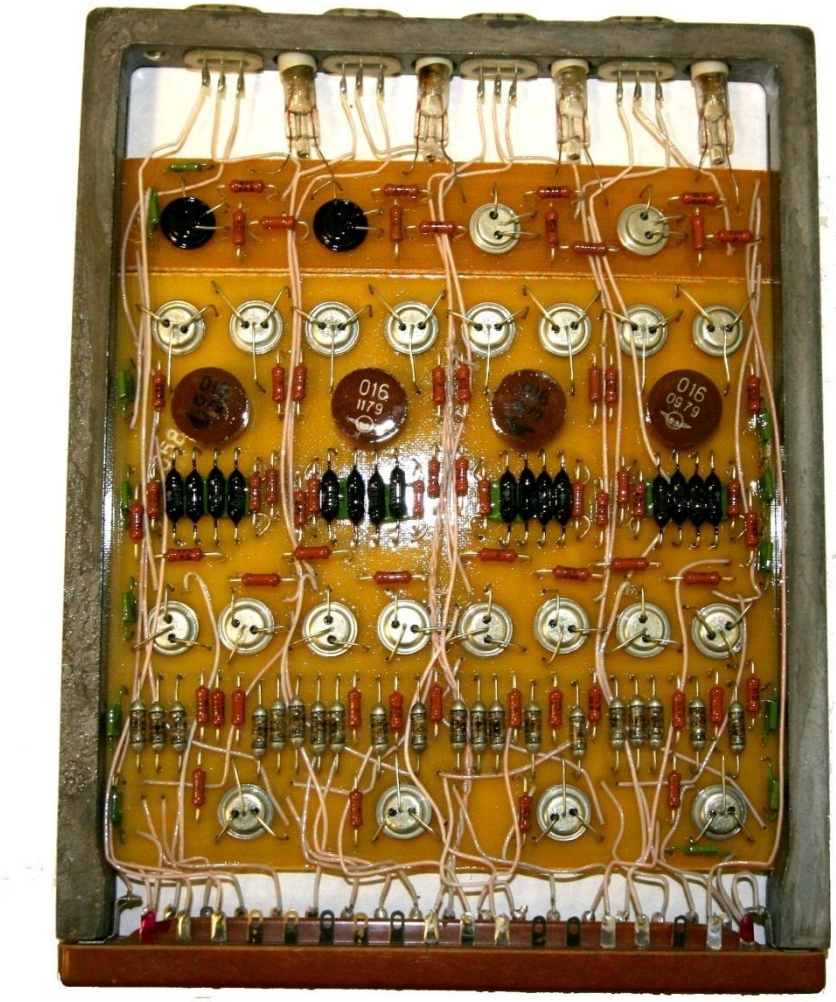

Fig. 6. У-block.