Test based on Built-In Current Sensors for Mixed-Signal Circuits

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Abstract. This paper presents a test methodology for mixed-signal circuits. The test approach uses a built-in sensor to analyze the dynamic current supply of the circuit under test. This current sensor emphasizes the highest harmonics of the dynamic current of the circuit under test when the current to voltage conversion is done. The goodness of the test method is analyzed first by means of a fault simulation and afterwards through the experimental data obtained from several benchmark circuits.

Keywords: Dynamic current test, Built-in current sensor, Design for test, Mixed–signal circuit

1 Introduction

The increase of mixed signal applications, with integrated circuits containing both analog and digital sections, motivates the development of design-for-test approaches for testing analog macros embedded in digital systems. The success of supply current monitoring (I_{DD}) in digital CMOS integrated circuits has prompted researches to investigate the feasibility of I_{DD} as a testing methodology for analog modules [1].

A survey of I_{DD} test methodologies, both quiescent and transient, can be found in [2]. All of them require precise measurements to be effective. Traditionally the current measurement is performed externally to the chip. However, to enhance the precision and to increase the sampling rate may require the use of suitable built-in current sensor circuits (BICS) to measure the current inside the chip [3].

The design of these BICS relies on the voltage drop across a resistance, induced by the dynamic supply current, in order to generate the fault signal. This current is captured in the sensor directly [4] or through current mirrors [5]. Sometimes, the charge accumulated in a capacitor is used to detect the shape of the dynamic current of the circuits with faults [6].

The paper is organised as follows. Section 2 highlights the contribution to technological innovation. Section 3 presents the I_{DDX} test method. Section 4 analyses the efficiency of the test method by means of a fault evaluation. Section 5 shows measured data from the benchmark circuits. Finally, the discussion and the conclusions are presented.

2 Contribution to Technological Innovation

This work proposes a new test method based on the analysis of the circuit dynamic current (I_{DDX}), both quiescent and transient, for the verification of digital, analog and mixed-signal circuits. The structural test method aims to reduce the test time and the complexity of the measurement equipment commonly used in mixed-signal tests.

3 Dynamic Current Test Method

In order to process accurately the information contained in the dynamic current that goes across the circuit under test (CUT), the measurement is performed by a built-in current sensor circuit (BICS) integrated within the CUT. Thus, it minimizes the distortion effect of the capacitances and inductances associated with the input/output pads, the circuit package and the elements of the printed circuit board.

The BICS output provides a sequence of digital pulses whose width reflects the amplitude and duration of the dynamic current. Defective circuits are exposed comparing the BICS output waveform of the CUT with the expected one for the fault-free circuit.

The test setup, besides providing the CUT stimulus, requires a digital signature analyzer to process the BICS output. This low cost equipment can be as simple as an integrator, a counter or a memory.

3.1 Built-In Current Sensor

In the mixed signal circuit, the current across the digital logic is sampled in series by a BICS placed in the power supply path between the CUT ground (Virtual_GND) and the chip pin (GND) (figure 1). The sampling element is a MOSFET transistor because it is able to accept large current transients without introducing a significant voltage drop and, at the same time, it is sensitive to the small quiescent currents [7].

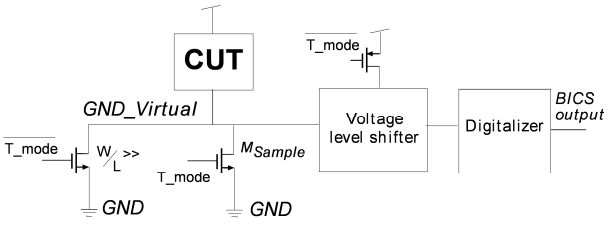

Fig. 1. BICS to analyse the dynamic current through the digital logic.

However, this measurement strategy would degrade the performance of the analog blocks due to the reduction of their effective voltage supply. Therefore, in this case, the current is replicated by placing additional branches to the current mirrors of the

circuits, taking advantage of the widely use of these basic build blocks in analog design [8].

In both cases, the sampled current is converted to voltage, then amplified and finally digitalized by a window comparator made of CMOS digital gates.

Under faulty conditions, the normal values of the analog circuit current may be increased, decreased or more generally distorted. Some of these faults do not produce a significant change in the quiescent current. However, they can affect the relationship of the harmonic components of the current waveform, causing a change in the slope of transient of the dynamic supply current [9].

So, we have designed a novel built-in current sensor circuit with the goal to emphasize the high-frequency components of the current when the current to voltage conversion is done. It uses the principle that a capacitor placed at the output port of a gyrator behaves like an inductance at the input port.

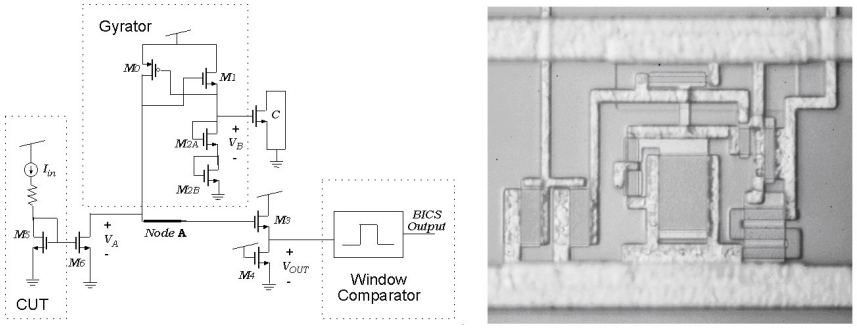

Fig. 2. Proposed Built-In current sensor (a) Scheme and (b) die photograph.

The circuit relies on the inverted back-to-back connection of active devices to implement the basic gyrator behaviour. The transconductance sources are done with two transistors, an NMOS (M0) and a PMOS (M1), connected as it is shown in figure 2a. Transistors M2 bias M0 and M1 in the saturation region. The capacitor (C) is achieved by means of the gate capacitance of another NMOS transistor [10].

A prototype, without the window comparator, has been fabricated with the Austria MicroSystem (AMS) 0.6 µm technology to characterise the frequency response of the circuit. The chip photograph can be seen in figure 2b.

Figure 3 displays the experimental measurements of the circuit tranresistance (v_{OUT} vs. i_{IN}). The left graph shows a good agreement among the theoretical calculus using the small signal model of the circuit, the layout simulation with the AMS 0.6µm technological transistor models and the data measured from a fabricated chip.

The circuit behaviour emulates an inductance with one series and one parallel stray resistor, where the BICS sensitivity to the high frequency components of the current can be appreciated in the abrupt change of the circuit output voltage (lower graph of figure 3b) when a current pulse is injected at the BICS input (upper graph of figure 3b). The quiescent change of the voltage, after the current stabilization, is smaller and it is given by the low frequency impedance of the circuit.

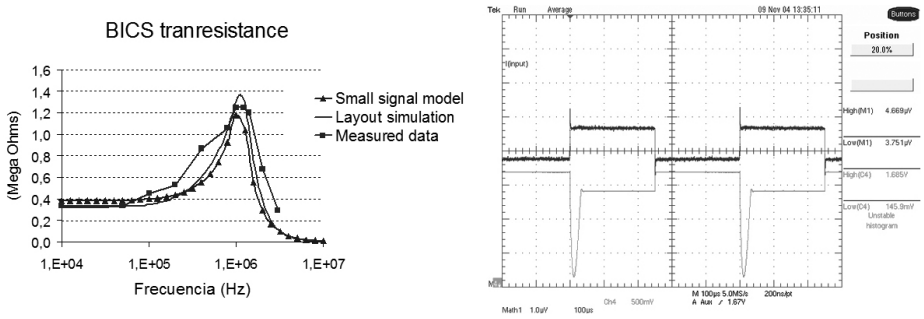

Fig. 3. BICS tranimpedance measure: (a) frequency and (b) transient responses.

The BICS design is quite sensitive to process spread attributable to the transistor implementation of the capacitor.

4 Fault Evaluation

A fault simulation has been carried out to check the efficiency of the test method. The process consists on the analysis of CUT behaviour when we include the electrical abstraction of a fabrication defect (known as fault) and the comparison of the circuit performance with expect for the fault-free one.

Defects in the integrated circuit materials commonly give rise to catastrophic faults [11]. In this work, we have considered short circuits between the transistor terminals, gate oxide shorts (GOS) and large deviations of the passive components (figure 4).

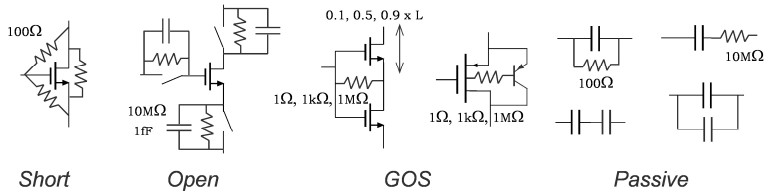

Fig. 4. Catastrophic transistor fault model.

The fault model includes soft opens due to cracks in the interconnection lines, where there is still a small current flow due to the quantum phenomenon of the tunnel effect. Hard opens, especially the open gate defect, due to the complete disconnection of the line strongly depends on the technology and physical topology of the circuit and are more difficult to model in an initial stage of the circuit analysis [12].

The I_{DDX} test method uses the width of the digital pulses that appear at the sensor output for each transition of the CUT inputs to expose the defective circuits. In order to get an estimation of the goodness of the proposed test approach, the fault coverage obtained through the BICS output is compared with other more traditional structural

tests. They are the quiescent current (I_{DDQ} test) and the DC voltage at the circuit outputs.

The threshold detection limit can be established through a Montecarlo simulation taking into account the process spread, or by means of the comparison with the measures taken from a well-known good circuit (golden device). These limits include a 100ns resolution in the pulse width of the BICS digital output, a 5µA variation in the I_{DDQ} of the CMOS logic, a change in the logic state of the digital outputs, and a 10mV deviation for the expected voltage at the analog block output.

Several benchmark circuits, both digital and analog, have been designed and fabricated to carry out the test evaluation. The digital module includes combinational logic cells and sequential memory registers. The BICS is placed between the CUT ground and the ground package pin [13].

The analog block is an operational amplifier in a voltage follower configuration. The current through the differential stage of the operational amplifiers is sampled by a new transistor added to the current mirror. As these circuits are usually connected in feedback configurations, the sampled current is sensitive not only to the differential stage and the bias network but also to the output stage.

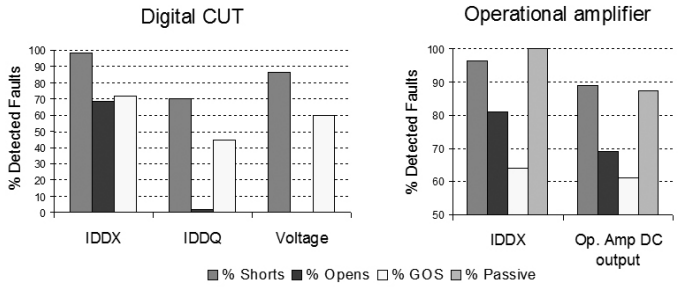

Fig. 5. Fault coverage of the digital logic and the operational amplifier.

Figure 5 shows the fault coverage obtained in the test evaluation. The detected faults are classified according to their type (shorts, opens, GOS and passive components) and the detection methodology applied. Our dynamic current test approach is shown in the left hand columns (I_{DDX}) and the reference structural tests in the right ones. Quiescent current (I_{DDQ}) and voltage test (*Voltage*) for the digital logic together with the operational amplifier DC output voltage (*Op. Amp. DC output*).

It can be appreciated a larger fault coverage from the I_{DDX} method. The reason is that some faults are detected through the change in the duration of the transient current in spite of not modifying the quiescent current or the DC voltage of the CUT (I_{DDQ} *or DC Voltage*) [8][9].

5 Experimental Measurements

The test method has been experimentally validated through the design and fabrication of the benchmark circuits with the implementation of the BICS.

Figure 6 shows a measure of the BICS that analyzes the current through the digital logic. The sensor generates pulses proportional to the CUT dynamic current when a transition happens at the circuit inputs or at the clock signal.

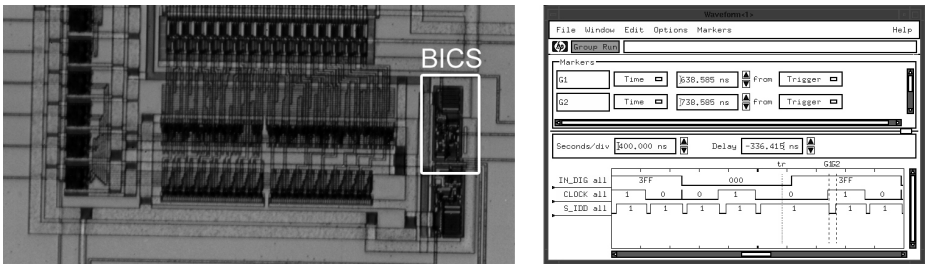

Fig. 6. Digital logic and BICS (a) chip photograph and (b) measured waveforms.

Three faults have been integrated within the manufactured operational amplifier (figure 7). All the faults have a parametric behaviour as they are implemented by an NMOS transistor (W=1μm, L=80μm) whose ON resistance is over 250 KΩ. The faults emulate a mismatch on the current mirror transistors of the differential stage (F1), an oxide pinhole in the compensation capacitor (F2) and a deviation in the current provided by the bias network (F3). An analog multiplexer selects each time a fault.

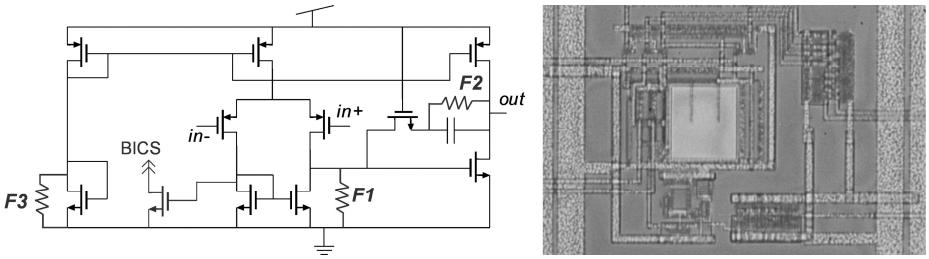

Fig. 7. Operational amplifier with injected faults (a) schematic and (b) chip photograph.

The operational amplifier is configured as voltage follower in this experiment. The input and the output voltages are displayed on the upper part of figure 8 graphs for the fault-free and two faulty conditions. The BICS waveforms are displayed on the lower part of figure 8 graphs. Although the three faults produce small variations on the DC levels at the operational amplifier output, almost negligible in F3, all of them induce a large change in the pulse width of the BICS, consequently they are easily detectable with the proposed test method [14].

The same measured values for gain, offset voltage and slew-rate in two versions of the operational amplifier, one alone and the other with the BICS, allows appreciating the minimal influence of the sensor in the CUT performance.

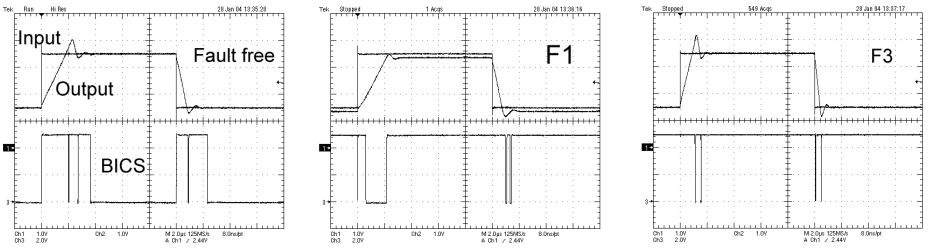

Fig. 8. Measured waveforms of the CUT and BICS output.

The influence of the process spread in the BICS behaviour can be notice in table 1. It shows the Montecarlo simulation of the fabricated circuit. The large standard deviation of the BICS pulse width has to be taken into account to set the boundary limits for the pass/fail flag. To obtain these values it may be necessary to know precisely the fabrication parameters or to use a golden device as reference. In spite of this dispersion, the BICS output allows a clear discrimination between the fault-free circuit and the defective ones.

Table 1. Montecarlo simulation of the pulse width of the BICS output.

BICS Output	Typical value	Mean value	Standard deviation
Fault free	2.67 us	3.28 us	1.46 us
F1	18.85 us	15.86 us	5.82 us
F2	13.29 us	12.58 us	2.61 us
F3	19.84 us	19.66 us	0.81 us

6 Discussion of Results

The proposed I_{DDX} test method provides a better fault coverage figure than the one obtained from a more traditional structural DC tests used as reference. Although, sometimes it is still necessary to characterize the functional performance of the mixed signal circuits before shipment due to customer or manufacturer necessities, the reduced test time and lower requirements of the test equipment makes this structural I_{DDX} test suitable for its application at the wafer level allowing an easy discrimination of the chips before their inclusion in the system package.

7 Conclusions and Further Work

This work proposes a new test method for mixed-signal circuits based on the analysis of the circuit dynamic current (I_{DDX}), both quiescent and transient.

The structural test uses a built-in current sensor to sample the dynamic current through selected branches of the CUT. The BICS was designed to prioritise the information obtained from the highest frequency components of the current.

The future development of this work should study the correlation between the BICS output and the functional performance of the CUT to relate the structural fault detection of the proposed I_{DDX} test with the test process yield.

The test method can be extended to a full BIST structure. To achieve this, the output signal processing must be included within the chip. It will be also necessary to allow the user to set the threshold limit that classifies the circuit as defective and to standardize the communication between the BICS and the test system.

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