Design Method and Implementation of Ternary Logic Optical Calculator

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Abstract

Compared with the conventional electronic computer, the Ternary Optical Computer (TOC) is the better idea for next generation computing tools because it possesses numerous data bits, enough intercom bandwidth, and inter controller made of electronic computer, but when designing optical calculators in TOC, there is much randomness that bring the manufacture of the optical calculators on lots of difficulties. In order to clear up the randomness, we have analyzed various designs of the optical calculators. In this research, a new rule, named the Decrease-Radix Design, was founded. According to the rule we established a design criterion for multi-valued logic calculator which includes eight steps. According to the criterion, all ternary logic optical calculators can be designed by a few basic units and the calculators have clear structures. It is possible to reconstruct any ternary logic optical calculator with the same basic units group by virtue of the criterion. Followed the design criterion, a hundreds-bit reconfigurable ternary logic optical calculator has been designed till June, 2007. In this paper we introduce the Decrease-Radix Design rule and the design criterion of multi-valued logic calculator in detail, and also introduce the design, manufacture and the experiment of the hundreds-bit reconfigurable ternary logic optical calculator. In the end, some photos of the optical calculator and its experiment will be shown.

[Keyword] Design Criterion, Ternary Logic, Reconfigurable, Ternary Optical Computer, Optical Calculator

1. Introduction

The Ternary Optical Computer(TOC) Principle [1][2][3][5][11], presented by Prof. Yi Jin in 2002, in which information was expressed with no light state and two perpendicular polarization directions light (such as the vertical polarization light and the horizontal polarization light) and the three optical states can be transformed each other using liquid crystal and polarizer, is a bran-new idea for next generation computing tools because that it possesses of numerous data bits, enough intercom bandwidth, and inter controller made of electronic computer. After that, lots of experiments on TOC were conducted. The researchers in this area have carried out a series of experiments on the design and the manufacture of some important components, i.e. the ternary optical encoder [8][9][10], ternary optical decoder [8][9], ternary logic optical calculator [7], ternary optical half-adder and full adder [4][6], and tried to develop the corresponding ternary optical computer prototype. But when designing optical calculators in TOC, there is much randomness. Commonly, the designs of optical calculators completely depend on inspiration of designers, so it is possible that different light diagrams are gained by different designers. All these not only make the design of light diagram of optical calculator slow but also make the design quality ensured difficultly; in addition, they also bring the manufacture of the optical calculators on lots of difficulties. These disadvantages are obvious in the development of the ternary logic optical calculators.

In order to solve these problems, a design criterion of multi-valued logic calculator [15][16] was presented and was applied to the manufacture of ternary logic optical calculators in this paper. According to the criterion, all ternary logic optical calculators can be designed by a few basic units and the calculators have clear structures. It is possible to reconstruct any ternary

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logic optical calculator with the same basic units group by virtue of the criterion. Followed the design criterion, we have designed and set up a hundreds-bit reconfigurable ternary logic optical calculator in June, 2007. In this paper we introduce the design criterion of multi-valued logic calculator in detail, and also introduce the design, manufacture and the experiment of the hundreds-bit reconfigurable ternary logic optical calculator.

2. Decrease-Radix Design Rule [15][16]

The operational capability of n-valued logic calculator with two inputs can be defined by the truth table of input and output. This truth table is n×n array in which the element lies in i row and j column is denoted by c_{ij}. And each n-valued calculator must have n different physical states to represent these n values. In order to discuss conveniently, some symbolic definitions are given as follows:

(1) Use τ_i to represent information, and all τ_i assemble the set i.e. $\Omega=\{\tau_1, \tau_2, \ldots, \tau_i, \ldots, \tau_n | i=1,2,\ldots,n\}$.

(2) Use λ_i to represent physical state, and all λ_i assemble the set i.e. $\Phi=\{\lambda_1, \lambda_2,\ldots, \lambda_i, \ldots, \lambda_n | i=1,2,\ldots,n\}$.

(3) $LT_k(n)$(k=1,2,…,n) represents a truth table of n-valued logic, in which all the elements c_{ij} belong to the set Ω.

(4) $PT_k(n)$ (k=1,2,…,n) represents a truth table of n-valued logic, in which all the elements c_{ij} belong to the set Φ.

Definition 1: If the result is still λ_i when one physical state in set Φ overlaps with $\lambda_i(\in\Phi)$, the physical state is called the **state D**. It is possible that there is no the state D in the set Φ, but it is also possible that there are several states D in the set Φ.

Definition 2: If only one element in the truth table $PT_k(n)$ is not the state D, then this truth table PT_k(n) is called the basis-element table $BT_k(n)$ (k=1,2,…,n).

Only one element in $BT_k(n)$ is not the state D and the other (n×n-1) elements are the state D, then the $BT_k(n)$ is a n×n two-value table. Due to there are (n-1) physical states in the set Φ which are not the state D, there are (n-1) basis-element tables which have one element that is not the state D at the same position; furthermore, there are n×n positions of element in the $BT_k(n)$, thus the number of basis-element table is n×n×(n-1) totally.

2.1. Select physical states

In principle, the steady physical state which can be transferred from one state to another by apparatus can be used to represent information. Therefore there are many optional schemes of the set Φ, in which those schemes that can generate such set Φ which contain the state D are the discussion object of this paper, and these schemes can be used to implement multi-valued computer system conveniently.

For example, the wavelength, intensity and polarization direction of light signal can all be used to represent information, in which the no light state is the connatural state D because that when it overlaps with any light signal which have any wavelength, any intensity and any polarization direction, the no light state seems nonentity to the result of the overlap, so it accords with definition 1. If the no light state, vertical polarization light and horizontal polarization light are selected to represent information in one system i.e. Φ= {no light state, vertical polarization light, horizontal polarization light}, there lies the state D (no light state), so the design criterion presented in this paper can be used to complete corresponding design task easily and conveniently. And if only the vertical polarization light and horizontal polarization light are selected to represent information in a system i.e. Φ={vertical polarization light, horizontal polarization light}, there is not the state D for neither the vertical polarization light fall short of definition 1 nor the horizontal polarization light. This is not the domain of this paper.

2.2. Mapping between physical states and information symbols

Commonly, the operational capability of logic calculator is given by the corresponding truth table $LT_k(n)$ in which the element is a information symbol, but the implement of it must depend on the physical states transfer. So firstly, the element mapping relationship between physical state set Φ and information symbol set Ω must be defined. There are (n!) optional mapping relationships totally, but different mapping relationship corresponds with different complexity of logic calculator structure. In this paper, using the state D to represent the information symbol which is the most frequently appeared in $LT_k(n)$, in this way, the final structure of logic calculator is most simple.

2.3. Derive from $PT_k(n)$

The truth table $PT_k(n)$ can be derived as following steps:

(1) Select an element c_{ij} which value is not the state D from $PT_k(n)$.

(2) Construct an n×n array truth table in which all elements are the state D.

(3) Replace the element of n×n array truth table in step (2) which lies in i row and j column with the element c_{ij} in step (1). According to definition 7, this

truth table (n×n) replaced is a basis-element table $BT_k(n)$.

(4)Repeat step (2) and step (3) for every element c_{ij} in $PT_k(n)$ which value is not the state D.

After the above four steps, some different basis-element tables $BT_k(n)$ can be derived from the truth table $PT_k(n)$, and the number of basis-element table $BT_k(n)$ is the same as the number of the element in truth table $PT_k(n)$ which value is not the state D. Considering the invariability of physical states overlap with the state D and the rule of matrix addition, the $PT_k(n)$ can be obtained by the "addition"of all derived $BT_k(n)$. This "addition" is not pure addition operation of mathematical matrix for the base of the "addition" is the invariability of physical states overlap, so it is called **DH operation**. The another meaning of DH operation is that the $PT_k(n)$ can be divided into the seriate DH operation expression of all derived $BT_k(n)$.

Definition 3: The device that can realize overlap processing of physical states is called **overlapper**.

Each truth table corresponds to a calculator, and the calculator corresponding to basis-element table $BT_k(n)$ is called basis-element calculator. If overlap the output state of these basis-element calculators using overlapper, then a multiplex calculator can be obtained. It is obvious that the function truth table of the multiplex calculator is the $PT_k(n)$.

A n-valued calculator has n-valued input and output. But because one basis-element calculator has a n-valued input and a two-value output, so the construction of basis-element calculator is simpler than that of n-valued calculator, and it can be realized easily. If the construction of overlapper is simple, then any n-valued logic calculator can be obtained by the combination of several simple basis-element calculators using simple overlapper. This design rule is called Decrease-Radix Design.

3. Design Criterion of multi-valued logic calculator

According to the above rule of Decrease-Radix Design, the design criterion of n-valued logic calculator is given as follows:

(1) Give the truth table $LT_k(n)$ of n-valued logic calculator ready to design.

(2) Select the state D and overlapper.

(3) Using the state D to represent the information symbol which is the most frequently appeared in $LT_k(n)$.

(4) Mapping between the other (n-1) physical states and the remainder (n-1) information symbols freely.

(5) Write the truth table $PT_k(n)$ corresponding to the $LT_k(n)$ using the mapping relationship selected by step (3) and step (4).

(6) Derive from the $PT_k(n)$ according to the steps in section 2.3, some $BT_k(n)$ will be obtained.

(7) Design the basis-element calculators corresponding with the $BT_k(n)$ obtained in step (6).

(8) Construct the n-valued logic calculator by overlap the output of every basis-element calculator designed in step (7) using overlapper.

Table 1 truth table $LT_k(3)$ of one ternary logic

Output c		Input a		
		0	m	1
Input b	0	0	m	m
	m	m	m	m
	1	m	m	1

For example, the no light state, vertical polarization light and horizontal polarization light (Denoted by W, V and H in the following tables) are selected to represent the ternary information in the system of TOC, and the no light state is the state D. Supposing that the truth table of one ternary logic is shown in Table 1, then the corresponding ternary logic optical calculator can be designed according to the above design criterion, as follows:

Step 1: Write the truth table $LT_k(3)$ of the ternary logic, shown in Table 1.

Step 2: The no light state is the state D, and select the half-reflect and half-transmission mirror as the overlapper.

Step 3: Use the no light state (state D) to represent m which is the most frequently appeared in Table 1.

Step 4: Use the horizontal polarization light (H) to represent 0 and vertical polarization light (V) to represent 1.

Step 5: Write the truth table $PT_k(3)$ corresponding to the $LT_k(3)$, shown in Table 2.

Table 2 $PT_k(3)$

Output c		Input a		
		W	V	H
Input b	W	W	W	W
	V	W	V	W
	H	W	W	H

Step 6: Derive from the $PT_k(3)$ according to the steps in section 2.3, as follows:

(1) Select the element c_{22}=V from Table 2.

(2) Construct a truth table (shown in Table 3) in which all elements are W (the state D).

Table 3 truth table (3×3)

Output c	Input a

		W	V	H
Input b	W	W	W	W
	V	W	W	W
	H	W	W	W

(3) The basis-element table $BT_m(3)$(shown in Table 4) is derived by replace the corresponding element of Table 3 with the element c_{22} selected in step (1). As the input a1 and b1 in Table 4 are the beam splitting from the input optical path a and b in Table 3 respectively, so a1=a, b1=b.

Table 4 $BT_m(3)$

Output c1		Input a1		
		W	V	H
Input b1	W	W	W	W
	V	W	V	W
	H	W	W	W

(4) Select the element c_{33}= H from Table 2.

(5) Construct a truth table (shown in Table 3) in which all elements are W (the state D).

(6) The basis-element table $BT_n(3)$(shown in Table 5) is derived by replace the corresponding element of Table 3 with the element c_{33} selected in step (4). As the input a2 and b2 in Table 4 are the beam splitting from the input optical path a and b in Table 3 respectively, so a2=a, b2=b.

Table 5 $BT_n(3)$

Output c2		Input a2		
		W	V	H
Input b2	W	W	W	W
	V	W	W	W
	H	W	W	H

Step 7: Design basis-element calculators (shown in Figure 1 and Figure 2) corresponding with the $BT_m(3)$ and $BT_n(3)$ respectively. In Figure 1 and Figure 2, a1,a2,b1 and b2 are the input optical path, c1 and c2 are the output optical path, v1,v2 and v3 are the polarizer that only permit vertical polarization light pass(Denoted by vertical polarizer in following part), h1,h2 and h3 are the polarizer that only permit horizontal polarization light pass(Denoted by horizontal polarizer in following part), LC1 and LC2 represent the liquid crystal unit which disable the optical rotation when the input optical path of light controller is not the no light state, the broken line represents the input optical path of light controller. The working principle of Figure 1 is: a closed light valve consists of v2, v3 and LC1, when input a1 is the horizontal polarization light or no light state, no light can pass through v1, the LC1 rotates light, then the valve closed and output c1 is no light state whatever the input b1 is. When the input a1 is the vertical polarization light which can pass v1 and LC1 disable

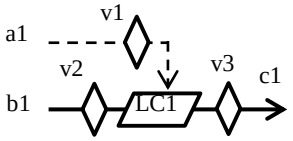

Figure 1 Basic operation unit corresponding to $BT_m(3)$

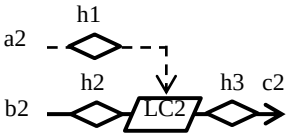

Figure 2 Basic operation unit corresponding to $BT_n(3)$

optical rotation, then the light valve can let the vertical polarization light pass. At the same time, if the input b1 is also the vertical polarization light, then it can pass through light valve to output c1, so c1 outputs the vertical polarization light. If the input b1 is not the vertical polarization light, for b1 cannot pass through light valve, c1 outputs the no light state. The conclusion can be obtained here that it is only when a1 and b1 are the vertical polarization light at the same time c1 can output the vertical polarization light, otherwise c1 outputs the no light state. So light diagram in Figure 1 realizes the $BT_m(3)$. The workong principle of Figure 2 is similar to that of Figure 1, only when a2 and b2 are the horizontal polarization light at the same time, c2 can output the horizontal polarization light, otherwise the no light state. That is, light diagram in Figure 2 realizes the $BT_n(3)$.

Step 8: The final structure of this ternary logic optical calculator shown in Figure 3 is the result of overlapping the outputs of c1 in Figure 1 and c2 in Figure 2 into one output light path c using the overlapper f(here is the half-reflect and half-transmission mirror). The symbols in Figure 3 are the same as those in Figure 1 and Figure 2. The working principle of Figure 3 is similar to that of Figure 1, when a1,a2,b1 and b2 are the vertical polarization light at the same time, c can output the vertical polarization light,

when a1,a2,b1 and b2 are the horizontal polarization light at the same time, c can output the horizontal polarization light. Otherwise the output c is the no light state. So light diagram in Figure 3 realizes the $PT_k(3)$.

To any ternary logic, so long as there is the

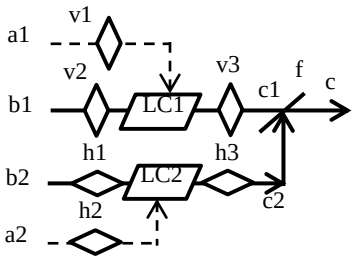

Figure 3 Final structure of optical calculator

corresponding truth table, the corresponding normative ternary logic optical calculator can be designed step by step according to the above method.

4. Implementation of hundreds-bit reconfigurable ternary logic optical calculator

Carrying out ternary logic operation directly is one of the characters of the tenary optical computer. And ternary optical half-adder, ternary optical full adder, ternary optical multiplier and other important components are all based on ternary logic operation. So the implementaion of a well-designed ternary logic optical calculator is the precondition of the ternary optical computer prototype, and its capability and bulk determine the future ternary optical computer's capability and bulk directly.

The advantage of above design criterion is using comparatively simple basis-element calculators to "assemble" various logic calculators. This character make the reconfiguration on the hardware of the ternary logic optical calculator is possible. A hundreds-bit reconfigurable ternary logic optical calculator is implemented using the apparatus which is current in market, such as liquid crystal display, polarizer, embeded system etc. and VC etc. developing eviroments in this paper. The following introduces the design, manufacture and the experiment of this reconfigurable calculator in detail.

4.1. Design of basis-element calculator

According to definition 2, it can be concluded that there are $3\times3\times(3-1)=18$ basis-element tables $BT_k(3)$ in ternary logic optical calculator. These $BT_k(3)$ and corresponding basis-element calculators $A_k(3)$ (k=1,2,…,n) designed are shown in Table 6.

Table 6 18 $BT_k(3)$ and 18 $A_k(3)$

No.	$BT_k(3)$	$A_k(3)$
1	Table 1 in Appendix 1	Figure 1 in Appendix 1
2	Table 2 in Appendix 1	Figure 2 in Appendix 1
3	Table 3 in Appendix 1	Figure 3 in Appendix 1
4	Table 4 in Appendix 1	Figure 4 in Appendix 1
5	Table 5 in Appendix 1	Figure 5 in Appendix 1
6	Table 6 in Appendix 1	Figure 6 in Appendix 1
7	Table 7 in Appendix 1	Figure 7 in Appendix 1
8	Table 8 in Appendix 1	Figure 8 in Appendix 1
9	Table 9 in Appendix 1	Figure 9 in Appendix 1
10	Table 10 in Appendix 1	Figure 10 in Appendix 1
11	Table 11 in Appendix 1	Figure 11 in Appendix 1
12	Table 12 in Appendix 1	Figure 12 in Appendix 1
13	Table 13 in Appendix 1	Figure 13 in Appendix 1
14	Table 14 in Appendix 1	Figure 14 in Appendix 1
15	Table 15 in Appendix 1	Figure 15 in Appendix 1
16	Table 16 in Appendix 1	Figure 16 in Appendix 1
17	Table 7	Figure 4
18	Table 8	Figure 5

The basis-element table lies in No. 17 of Table 6, has an element which value is the vertical polarization light when two inputs are no light state. The corresponding calculator can not be realized by liquid crystal unit without lamp-houses. A method is presented to resolve the difficulty in this paper, as

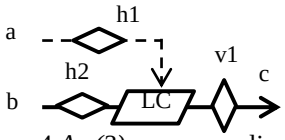

Figure 4 $A_{17}(3)$ corresponding to $BT_{17}(3)$

follows: change the physical states of inputs, that is, replace the no light state with the horizontal polarization light, and replace the horizontal polarization light with the no light state. The working principle of Figure 4 is similar to that of Figure 1, only when two inputs, a and b, are the no light state at the same time, and change to the horizontal polarization light, then c outputs the vertical polarization light, otherwise the no light state. Light diagram in Figure 4 with the above state changing method realizes the $BT_{17}(3)$ in Table 7. The basis-element table lies in No. 18 of Table 6 is similar to the above, it only need to replace the no light state with the vertical polarization light, and replace the vertical polarization light with the no light state.

Table 7 $BT_{17}(3)$

Output c	Input a		
	W	V	H

Input b	W	V	W	W
	V	W	W	W
	H	W	W	W

Changing the physical stats of inputs means the encoding method on the two basis-element calculator is

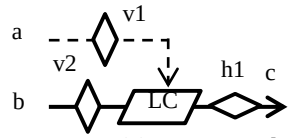

Figure 5 $A_{18}(3)$ corresponding to $BT_{18}(3)$

different with the others. Because the calculator and the corresponding encoder are determined before the beginning of data processing, the actual operation of encoder is choosing a corresponding coding method on these optical paths which are inputs of the two basis-element calculator. This will not add anything to the complexity of encoder. So this method is viable.

Table 8 $BT_{18}(3)$

Output c		Input a		
		W	V	H
Input b	W	H	W	W
	V	W	W	W
	H	W	W	W

4.2. Design and manufacture of the hardware part

Analyzing the structure of light diagrams of the

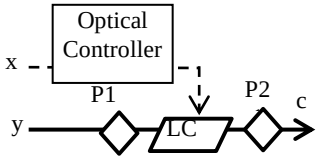

Figure 6 Representative structure of $A_k(3)$

eighteen basis-element calculators in Table 6, the representative structure can be abstracted (shown in Figure 6), as follows:

(1) There are two beam splittings: one is the main optical path y, the other is the control optical path x which disable or enable the optical rotation of liquid crystal unit LC.

(2) There is a liquid crystal unit LC in the main optical path y, the front and back sides of which has a polarizer respectively: P1 and P2.

(3) The liquid crystal unit LC is light controlled.

Nowadays, the technology of light controlled liquid crystal [12][13][14] is matured in the laboratory. But considering the process of TOC's research at present and the market of light modulator, at the condition that the principle can be validated by experiment, the selection of apparatuses needed abides by the principle that is the least spending of time and money. So the electronic controlled liquid crystal unit which is current in market is selected to replace the light controlled liquid crysta unit LC. Correspondingly, the optical controller is replaced with the electric controller, and Figure 6 is changed to Figure 7. The defect of this design is the low efficiency of the optical-electric-optical control used to realize the optical-optical control indirectly. For this detect will not effect the aim of the design and experiment, considering the advantages and the corresponding disadvantages, we choose this design.

For the function of optical controller in Figure 6 is realized by the function simulation of electric controller in Figure 7, the optical hardware of this

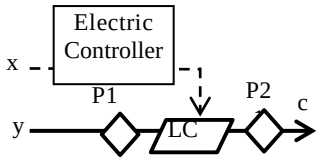

Figure 7 Representative structure of $A_k(3)$

system is only the main optical path y.

The electric controller in Figure 7 has an input which is ternary signals (the no light state, vertical polarization light and horizontal polarization light), and an out which is binary signals. The output signals are used to disable or enable the optical rotation of liquid crystal unit LC. In this paper, the symbol 0 represents the output signal which disables the optical rotation of LC, and the symbol 1 represents the output signal which enables the optical rotation of LC. The electric controller can realize 2^3=8 control logics, the corresponding truth table is C_1, C_2 … C7 and C_8, as shown in Table 9.

Table 9 8 truth tables of electric control logic

Output		Symbols of control logic							
		C1	C2	C3	C4	C5	C6	C7	C8
Input	W	0	0	0	0	1	1	1	1
	V	0	0	1	1	0	0	1	1
	H	0	1	0	1	0	1	0	1

There are two kinds of polarizer on the both sides of liquid crystal unit LC in the main optical path y: vertical polarizer and horizontal polarizer. Thus, the

hardware unit consisting of P1, LC and P2 has 2^2=4 different structures, as shown in Table 10.

Table 10 Types of optical hardware unit

Types Name	P1	P2
V-V	vertical polarizer	vertical polarizer
V-H	vertical polarizer	horizontal polarizer
H-H	horizontal polarizer	horizontal polarizer
H-V	horizontal polarizer	vertical polarizer

Then, according to Table 6, Table 9 and Table 10, the type name of hardware unit and the symbol of control logic which the eighteen basis-element calculators $A_k(3)$ of ternary logic optical calculator belongs to, can be listed in Table 11.

Table 11 Hardware unit types and electric control logic of $A_k(3)$

$A_k(3)$	Types name of hardware unit	Control logic name of electric controller
$A_1(3)$	V-V	C_4
$A_2(3)$	V-V	C_4
$A_3(3)$	V-H	C_5
$A_4(3)$	V-H	C_5
$A_5(3)$	H-V	C_5
$A_6(3)$	H-V	C_5
$A_7(3)$	H-H	C_4
$A_8(3)$	H-H	C_4
$A_9(3)$	V-V	C_6
$A_{10}(3)$	V-H	C_3
$A_{11}(3)$	H-V	C_3
$A_{12}(3)$	H-V	C_3
$A_{13}(3)$	V-H	C_2
$A_{14}(3)$	V-H	C_2
$A_{15}(3)$	H-V	C_2
$A_{16}(3)$	H-H	C_7
$A_{17}(3)$	H-V	C_2
$A_{18}(3)$	V-H	C_3

According to Figure 8 in which black areas represent the vertical polarizer, gray areas represent the horizontal polarizer and the white gridding middle area represents liquid crystal, adding corresponding

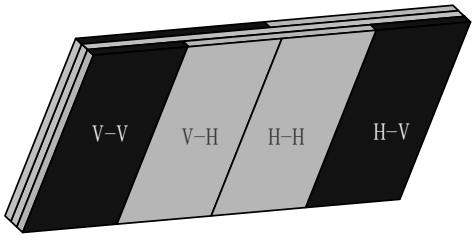

Figure 8 Allocation of polarizator

polarizers on two faces of a electronic controlled liquid crystal display array(type: YMSG-G12864P-12DYSWSN), then there are four separate areas in the liquid crystal array: area V-V, area V-H, area H-H and area H-V from left to right (shown in Figure 8). For the liquid crystal array has 64×128=8192 pixels, and each pixel can be used as one optical path, then there are 64×128=8192 optical paths totally and 64×128/4 = 2048 optical paths in each area. Considering the function stability of real system, it is necessary to use several pixels to represent one optical path redundantly. It is use 2×2=4 pixels as one optical path in this system, so there are 64×128/16=512 optical paths in each area, correspondingly the maximum data bits of the reconfigurable ternary logic optical calculator is 512 too. Thus the hardware part of the reconfigurable ternary logic optical calculator is completed, and the practicality photo is shown in Figure 1 of appendix 2. The system circuitry board made by ourselves is shown in Figure 2 of appendix 2, which supplies the hardware interface between liquid crystal module and embedded control chips, and realizes eight control logics in Table 9.

4.3. Architectures of experiment system

The whole architectures of experiment system is shown in Fighre 9, wherer R represents surface lamp-house, C represents coder, P represents the hundreds-bit reconfigurable ternary logic optical calculator completed in section 4.2, D represents decoder, L represents homogenized beam of light, and S represents data stream.

The coder C realizes the data stream S represented with light state by modulating from homogenized beam of light L to ternary information beams. The working principle of C was introduced in Reference 11. The decoder D is a light-electron conversion device which can convert the ternary light information to binary electronic information.

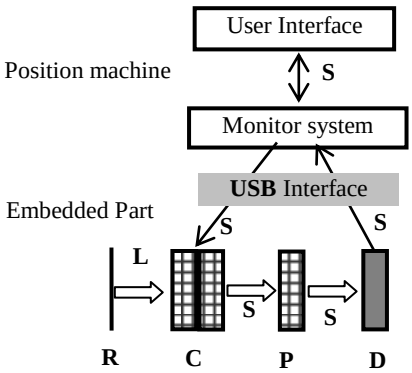

Figure 9 System whole architectures

The software of this system includes two parts: position machine and embedded part. The two parts

can communicate with each other through USB interface. The position machine provides user interface, operation window, USB device driver and a simple monitor system which can realize the dynamic hardware reconfiguration of the hundreds-bit reconfigurable ternary logic optical calculator, simulation display and analysis of experiment result. The embedded part controls and synchronizes coder C, logic calculator P and decoder D.

Partial figures of software interface are shown in appendix 2.

4.4. Process and result of experiment

There is a software module in this system, which can realize the simulation display and analysis of current experiment results. So users can find errors visually in the operation interfaces directly, and the process of experiment is convenient and instant.

This system has carried out almost thousands of ternary logic operation during several months. The range of data bits used in operations is from severa to hundreds. The system is steady and reliable, and the operation results are acoup sur, which correspond with the expectant results totally. It can be concluded that the design criterion of multi-valuedlogic calculator presented in this paper is validity and efficient.

At present, this hundreds-bit reconfigurable ternary logic optical calculator has become a special demo system for visited and investigated. In this demo system, visitors can define any ternary logic freely, and the result of logic operation can be seen with either decoder or naked eyes when inputting any two hundreds-bit datum. Welcome anyone anytime visits the department of Computer, Shanghai University to investigate this system. The simpleness and efficiency of this system can make you surprised.

5. Conclusions

In this paper we present the design criterion of multi-valued logic calculators. The advantages of the design criterion are that any logic calculator can be formed with a few basic units which have simple structures. We have applied this method to the design of the ternary logic optical calculator and have set up a hundreds-bit reconfigurable ternary logic optical calculator successfully. All these promote an investigation on the key parts and the development of the Ternary Optical computer.

References

[1] Jin Yi, He Huacan, Lü Yangtian. Ternary Optical Computer Principle. Science in China (Series E), 2003,33(1): 111~115 (in Chinese)

[2] Jin Yi, He Huacan, Lü Yangtian. Ternary Optical Computer Principle. Science in China (Series F), 2003,46(2): 145~150 (in Chinese)

[3] Jin Yi. Ternary Optical Computer Principle and Architecture. PH D thesis, Northwestern Polytechnical University, 2002 (in Chinese)

[4] Jin Yi, He Huacan, Ai Lirong. Lane of Parallel Through Carry in Ternary Optical Adder. Science in China (Series F), 2005,48(1): 107~116 (in Chinese)

[5] Jin Yi, He Huacan, Lü Yangtian. Ternary Optical Computer Architecture. Physical Scripta,2005,T118: 98~101

[6] Jin Yi, He Huacan, AI Lirong. Lane of Parallel Through Carry in Ternary Optical Adder. Science in China (Series E), 2004,34(8): 930~938 (in Chinese)

[7] Jin Yi. Design and Experiment of Ternary Logic Optical Processor. Topical Meetings on optoinformatics, St. Petersburg, Russia, Oct.18~22, 2004:21~23

[8] Sun Hao, Jin Yi, Yan Junyong. Research on Principle of Coder and Decoder in Ternary Optical Computer by Experiment. Computer Engineering and Applications, 2004,40(16): 82~83,136 (in Chinese)

[9] Yan Junyong, Jin Yi, Sun Hao. Study on the Feasibility of Coding and Decoding Multi-bit Ternary Optical Signal Used in Ternary Optical Computer. Computer Engineering, 2004,30(14): 175~177 (in Chinese)

[10] Huang Weigang, Jin Yi, AI Lirong, et.al. Design and Implementation of the 100-Bit Coder for Ternary Optical Computers. Computer Engineering & Science Ptess,2006,28(4): 139~142 (in Chinese)

[11] Jin Yi, He Hua-can, Lü Yang-tian. Ternary Optical Computer Architecture. First International Meeting on Applied Physics, Badajoz, Spain, 14~18th, October 2003

[12] Khoo I C, Michael R R, Finn GM. Self-phase modulation and optical limiting of a low-power CO2 laser with a nematic liquid-crystal film, Appl. Phys. Lett., 1988, 52 (25) : 2108~2110

[13] Janassy I, Lloyd A D. Low-power optical reorientationin dyed nematics. Mol. Cryst. L iq. Cryst. ,1991, 203(5) : 77~84

[14] Janossy I. Molecular interpretation of the absorption-induced optical reorientation of nematic liquid crystals . Phys. Rev. E , 1994 ,49 (4) : 2957~2963

[15] Yan Junyong, Jin Yi, Zuo Kaizong. Decrease-Radix Design principle for carrying/borrowing free multi-valued calculator and application in Ternary Optical Computer. Sci China Ser F-Inf Sci, 2008, 51(10): 1415-1426

[16] Yan Junyong. Decrease-Radix Design Principle. PH D thesis, Shanghai University, 2009 (in Chinese)

Appendix 1 16 basis-element tables $BT_k(3)$ and corresponding basis-element calculators $A_k(3)$ in ternary logic optical calculators

In the following figures and tables, a and b are the input optical path, c is the output optical path, v1,v2 and v3 are the polarizer that only permit vertical polarization light pass, h1,h2 and h3 are the polarizer

that only permit horizontal polarization light pass, LC represents the liquid crystal unit which disable the optical rotation when the input optical path of light controller is the no light state, RLC represents the liquid crystal unit which disable the optical rotation when the input optical path of light controller is **not** the no light state, the broken line represents the input optical path of light controller, W is the no light state, V is the vertical polarization light, and H is the horizontal polarization light. The working principle of following figures is similar to that of figure 1 of the text.

Table 1 $BT_1(3)$

Output c		Input a		
		W	V	H
Input b	W	W	W	W
	V	V	W	W
	H	W	W	W

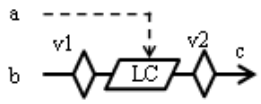

Figure 1 $A_1(3)$ corresponding to $BT_1(3)$

Table 2 $BT_2(3)$

Output c		Input a		
		W	V	H
Input b	W	W	V	W
	V	W	W	W
	H	W	W	W

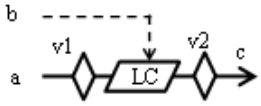

Figure 2 $A_2(3)$ corresponding to $BT_2(3)$

Table 3 $BT_3(3)$

Output c		Input a		
		W	V	H
Input b	W	W	W	W
	V	H	W	W
	H	W	W	W

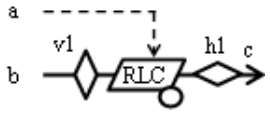

Figure 3 $A_3(3)$ corresponding to $BT_3(3)$

Table 4 $BT_4(3)$

Output c		Input a		
		W	V	H
Input b	W	W	H	W
	V	W	W	W
	H	W	W	W

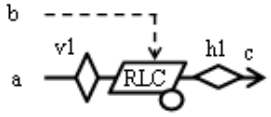

Figure 4 $A_4(3)$ corresponding to $BT_4(3)$

Table 5 $BT_5(3)$

Output c		Input a		
		W	V	H
Input b	W	W	W	W
	V	W	W	W
	H	V	W	W

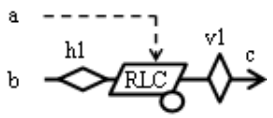

Figure 5 $A_5(3)$ corresponding to $BT_5(3)$

Table 6 $BT_6(3)$

Output c		Input a		
		W	V	H
Input b	W	W	W	V
	V	W	W	W
	H	W	W	W

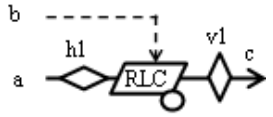

Figure 6 $A_6(3)$ corresponding to $BT_6(3)$

Table 7 $BT_7(3)$

Output c		Input a		
		W	V	H
Input b	W	W	W	W
	V	W	W	W
	H	H	W	W

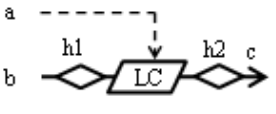

Figure 7 $A_7(3)$ corresponding to $BT_7(3)$

Table 8 $BT_8(3)$

Output c		Input a		
		W	V	H
Input b	W	W	W	H
	V	W	W	W
	H	W	W	W

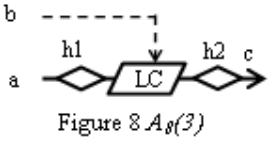

Figure 8 $A_8(3)$ corresponding to $BT_8(3)$

Table 9 $BT_9(3)$

Output c		Input a		
		W	V	H
Input b	W	W	W	W
	V	W	V	W
	H	W	W	W

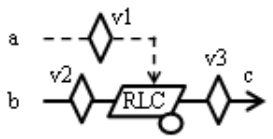

Figure 9 $A_9(3)$ corresponding to $BT_9(3)$

Table 10 $BT_{10}(3)$

Output c		Input a		
		W	V	H
Input b	W	W	W	W
	V	W	H	W
	H	W	W	W

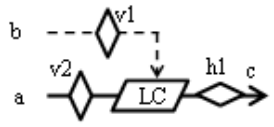

Figure 10 $A_{10}(3)$ corresponding to $BT_{10}(3)$

Table 11 $BT_{11}(3)$

Output c		Input a		
		W	V	H
Input b	W	W	W	W
	V	W	W	W
	H	W	V	W

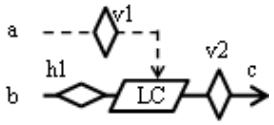

Figure 11 $A_{11}(3)$ corresponding to $BT_{11}(3)$

Table 12 $BT_{12}(3)$

Output c		Input a		
		W	V	H
Input b	W	W	W	W
	V	W	W	V
	H	W	W	W

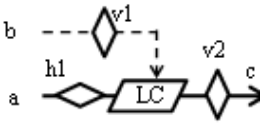

Figure 12 $A_{12}(3)$ corresponding to $BT_{12}(3)$

Table 13 $BT_{13}(3)$

Output c		Input a		
		W	V	H
Input b	W	W	W	W
	V	W	W	H
	H	W	W	W

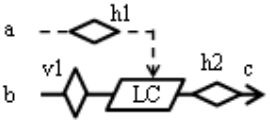

Figure 13 $A_{13}(3)$ corresponding to $BT_{13}(3)$

Table 14 $BT_{14}(3)$

Output c		Input a		
		W	V	H
Input b	W	W	W	W
	V	W	W	W
	H	W	H	W

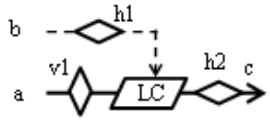

Figure 14 $A_{14}(3)$ corresponding to $BT_{14}(3)$

Table 15 $BT_{15}(3)$

Output c		Input a		
		W	V	H
Input b	W	W	W	W
	V	W	W	W
	H	W	W	V

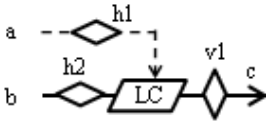

Figure 15 $A_{15}(3)$ corresponding to $BT_{15}(3)$

Table 16 $BT_{16}(3)$

Output c		Input a		
		W	V	H
Input b	W	W	W	W
	V	W	W	W
	H	W	W	H

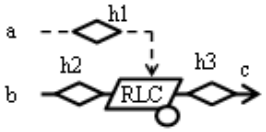

Figure 16 $A_{16}(3)$ corresponding to $BT_{16}(3)$

Appendix 2 Photos of hardware practicalities and software interface

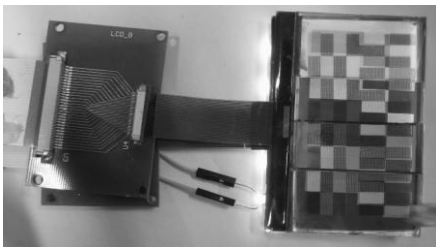

Figure 1 Photo of Hundreds-Bit reconfigurable optical calculator for ternary logic

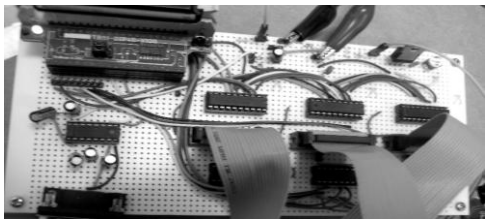

Figure 2 Photo of system Circuitry board

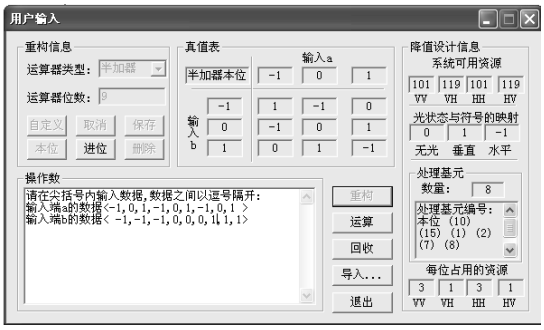

Figure 3 Window of user input

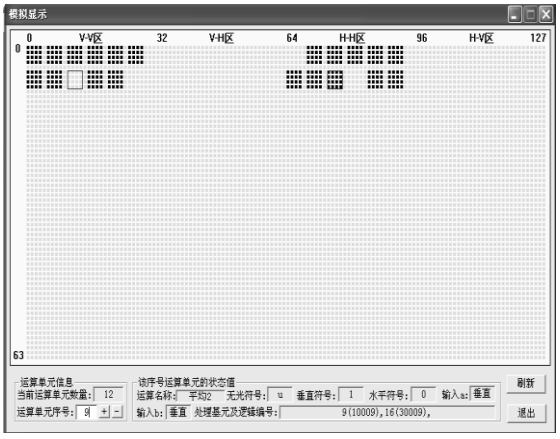

Figure 4 Window of simulation display