A Circuit Module and CPLD Laser Ground Controller Based on RS485

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Abstract :The function of the controller is to adjust the rise and fall of the ground shovel constantly according to the signal of positional deviation transmitted from the laser receiver, and remove or fill in the soil of the farmland, thus reaching the aim of smoothing the farmland. So the controller is the core component of the laser-control-ground system. The speed of response and the control algorithm of the controller are in relation to the stability and work efficiency of this system. This research uses the RS485 module to transmit, enhancing the interference immunity of the system, raising the stability when it works in severe environment, replacing SCM with CPLD to carry out the function of logical control, cutting down the power consumption of the system. It interferes manually in the hydraulic control automatic mode via software, thus improving the stability and flexibility of the system. The function of adjusting the duty cycle of the controller output signal is added, making the controller able to work both in paddy field and dry land.

Keywords：RS485 Circuit　CPLD　Laser Ground Controller

1. Introduction

The purpose of designing the controller is to achieve the matching of the controller with different types of hydraulic systems, and improve the controller's response to hydraulic actuator, carrying out the ground operation in different landforms (paddy field of dry land)[1]. Through the summary of large amount of previous ground operation, this research made some improvements upon the original controller. The signal transmission between the controller and receiver uses RS485 bus transfer mode instead of the previous current transfer mode, adding the function of manual interference in the rise and fall of the ground shovel under the automatic mode, carrying out the function of manual and automatic interlocking via software instead of the previous interlocking relying on gate circuit, simplifying the circuit's area and raising the circuit's stability; adding the function of adjusting the duty cycle of the controller output signal, thus adapting to different hydraulic mechanisms and different working landforms[2].

2. System Design for Hardware

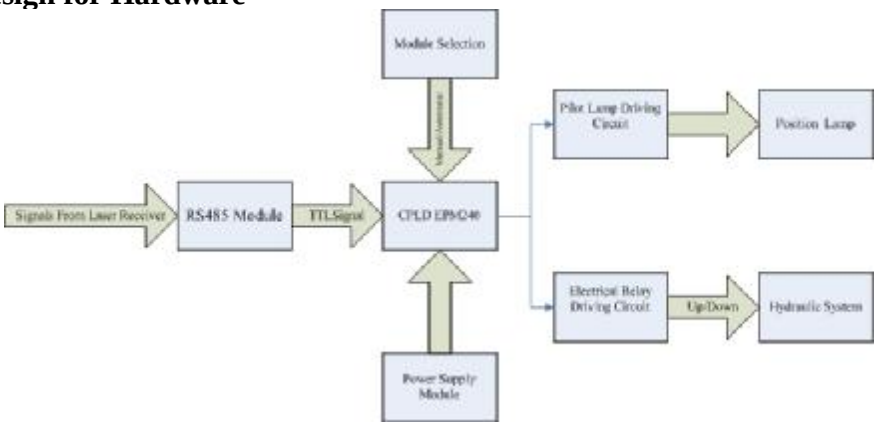


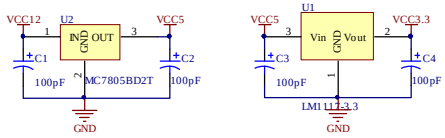
Figure 1 Hardware Structural of Controller

Figure 1 is the hardware structural of the controller. The receiver's signal is transmitted to the MAX485 circuit module of the controller via RS485 bus; MA485 converts the 485 electrical level to TTL level, then transmits it to CPLD to process; CPLD processes the position signal, then puts out the pilot lamp driving signal and hydraulic driving signal; the pilot lamp driving signal controls the on and off of the pilot lamp through the lamp driving circuit, displaying the level changes of the position; the hydraulic driving signal drives the hydraulic system to

work via controlling the relay switch, adjusting the rise and fall of the ground shovel. Users can choose between the automatic mode and manual mode for the system via the mode-selecting module.

3. Main Control Unit and Peripheral Circuit Design

This research uses the CPLD Chip EPM240T from Alteral Company as the main control chip. This chip has 240 logical units, 8K-bytes flash with the instant system programming function (ISP), making it very convenient to modify the system's function. The chip supports 300M clock frequency at the most; the maximum time delay between pins is 4.5 ns, providing more advanced property for users; 100 pins TQFP with smaller volume; 3.3V system voltage and 1.8V core voltage with lower power consumptio[13]n. CPLD programs' parallel processing is faster compared with 51 SCM, and the programs won't overflow; eliminating the peripheral devices like the Watch Dog, raising the stability and reliability of the system. Its inner unique structure fits well for disposing complicated combination logic circuit and sequential logic circuit. The power supply for the controller is from the tractor battery, with the voltage of 12V. The CPLD inside the controller needs a working voltage of 3.3V, and most chips like the pilot-lamp-driving circuit and the relay-driving module need a voltage of 5V, so it requires the power-supply-changeover module to convert the voltage from 12V to 5V and 3.3V. This research uses LM2575 power-supply-changeover chip to achieve the change from 12V to 5V, and uses LM117-3.3 to achieve the change from 12V to 3.3V. The power-supply-changeover circuit diagram is Figure 2. LM2575 is a kind of switching voltage regulator, with the features of small volume, high working efficiency, low heating value, etc. The maximum output voltage is 40V, maximum output current 1A, maximum voltage-stabilizing error 4%, with limiting-current circuit and overheating-protection circuit inside, etc. LM117-3.3 belongs to switching power-supply-changeover chips, with the features of heavy output current, high accurate output voltage, low ripple coefficient, etc. A tantalum capacitor of about 10u needs to be added to the outlet end of the power-supply-changeover when it is working, in order to filter the AC component in the direct voltage. And this research uses the electric relay to control the on-off of the power supply. VCC in Figure 3 is the power supply provided by the tractor's battery. When the switch S0 is on, the relay's normally open contact is on, out1 and out2 on, and the tractor's power supply accessed the controller.



(a) 12V to 5V Circuit (b) 5V to 3.3V Circuit

Figure 2 Power Convert Module of Controller

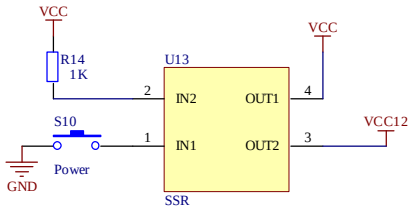


Figure 3 Power Switch of Controller

3.1 RS485 Circuit Module Design

RS-485 works in the way of half-duplex, with one sending and the other receiving. The position signal of the receiver is sent to the controller by RS-485 bus[14]. RS-485 uses the way of differential-level-receiving to raise the capability of anti-interference, fit for working under severe condition. The baud rate of the serial communication is 9600bit/s, and the data format is composed of 1 start bit, 8 data bits and 1 stop bit. The CPLD system uses MAX485 chip to accomplish the communication between the controller and receiver. As the system voltage for CPLD is 3.3V, MAX3485 is used to achieve the RS485 level changeover, and MAX3485 working under the power supply of 3.3V is a RS-485 changeover chip. As Figure 4 shows, Port A and B of MAX485 are linked to resistances, forming the differential voltage input; RO is the input end, and signals run into CPLD via RO when CON485 is linked to high electrical level. DI is the output end, and signals run out via DI when CON485 is linked

to low electrical level. As the controller only receives signals from the receiver, there is no need to send signals to the receiver, thus DI is not used. The MAX3485 chip has 8 pins, and their functions are as follows:

RO: Output end of the receiver, if A is 200mV higher than B, RO is high level; if A is 200mV lower than B, RO is low level.

RE: Strobe end of the receiver output. If RE is low, RO is effective; if RE is high, RO is in high-impedance state.

DE: Strobe end of the driver output. If DE is high, the driving output A and B are effective; if DE is low, they are in high-impedance state.

DI: Output end of the driver. If DI is low, it will force the output low; if DI is high, it will force the output high.

GND: Ground terminal.

B: Input of inverting receiver and output of inverting driver.

A: Input of inphase receiver and output of inphase driver.\

VCC: Positive electrode

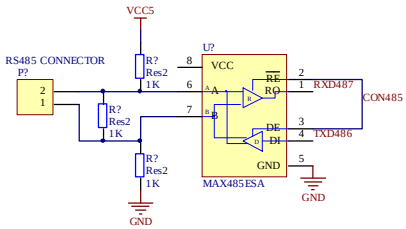


Figure 4 RS485 Communication Module

3.2 Hydraulic System Driving Circuit

The magnetic valve of the hydraulic system is controlled by the relay. One end of the normally-open-contact of the relay is connected with the electrical source, the other end with the magnetic valve. In order to improve the reliability of controlling the hydraulic system, this research uses solid state relay as the component for driving the hydraulic system. The solid state relay has a long operational life with high reliability. It is able to work under the circumstance of heavy impact and shock, because there is no mechanical part inside. At the same time, the solid state relay dose not have a input coil or contact arc or rebound, thus reducing the electromagnetic interference[15].

Figure 5 is the circuit of solid state relay driving hydraulic magnetic valve. CPLD controls the on-off of the relay via controlling the on-off of the transistor, thus carrying out the function of controlling the on-off of the hydraulic magnetic valve. For example, when the up port is high level, the Transistor Q1 is on; the Relay U11's normally open contact is closed (Port 4 and Port 3 are on), supplying power for the hydraulic system magnetic valve and driving the hydraulic system to lift the ground shovel. Likewise, when the down port is high level, the hydraulic system will lower the ground shovel. To prevent an excessive dash current when the relay is switched on, R3 is added as a current-limiting resistance. At the output end of the relay, an RC absorbing circuit is added, which can effectively restrain the transient voltage added to the relay and the exponential growth rate of the voltage. Also a piezo-resistor with given clamp voltage is linked to the output end, thus protecting the relay effectively[16].

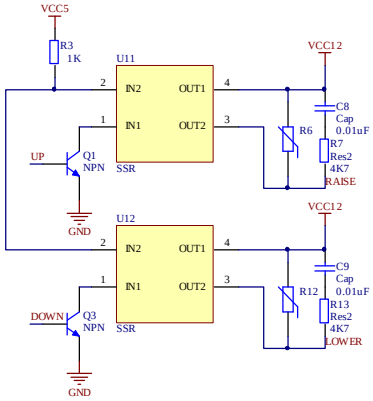


Figure 5 Hydraulic-System-Driving Circuit

3.3 Position Pilot Lamp Driving Circuit

The position pilot lamp can show the level of the ground of the time, which is convenient for users to conduct ground operations correctly accordingly. The controller makes judgment according to the information about position transmitted from the laser receiver, and then drives the transistors on or off, thus control the pilot lamp on or off. Figure 6 is the position pilot lamp driving circuit. The transistors used here are NPN 9013 low power transistors; the maximum working current of the collector is 500mA; the working temperature is from -55℃ to 150℃; the voltage drop between collector and base is around 0.3V when it is working in saturation region. The operational principle of the driving circuit: when the land level is higher than the reference plane, the receiver sends the position signal of the area to the controller; then the controller sends electrical level to HighLight port, Transistor Q6 conducted and LED5 on. There are 3 pilot lamps representing high, middle and low. So the information of the land level can be shown though the 3 lamps, providing the base of judgment for ground operation for users.

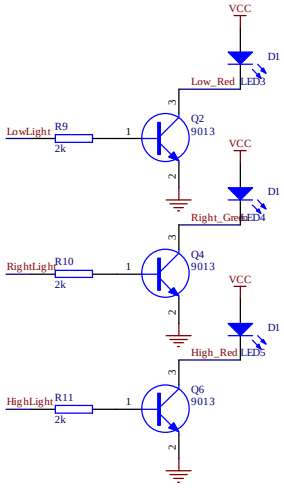


Figure 6 Position-Pilot-Lamp-Driving Circuit

4. Software Design Framework

This research uses VHDL hardware description language to program CPLD. The main functions of the controller are as follows: in the automatic mode, disposing according to the signals from the receiver, outputting driving signals for the hydraulic system and pilot lamp; in the manual mode, checking the signals from the rise button or the fall button, outputting controlling signals for the hydraulic system. The difficulty in the software design is to carry out UART serial function via hardware logical unit, receiving the serial data from the receiver, outputting hydraulic controlling signals whose duty cycle are adjustable, raising the speed of response and stability of the hydraulic system; the duty cycle of the hydraulic controlling signals from the controller can be selected artificially so that the controller can match different hydraulic systems and different ground shovel devices.

The receiver uses 36 photocells in all that are divided into 4 rows; each row includes 9 photocells, with 5 groups of signal inputs. The 5 groups of signals are amplified and reshaped through the circuit, and then are sent to Pin P2.0-P2.4 of the SCM; The SCM encodes the input signals, sends the data to Chip MAX485 through the serial interface, and to the controller through the signal wire after changing the TTL electrical level to 485 electrical level. The controller uses Chip MAX485 to transform the sent signals to TTL electrical level, and then sends it to CPLD to deal with.

In the laser receiver, every two contiguous photocells are 1.5mm apart, so there are two photocells at most receiving laser signals at the same time, thus there are 9 effective states for the 5 groups of input signals. Table 1 is the signal codes for effective states of the laser receiver and the controlling signals' frequencies and duty cycles from the controller to the hydraulic system.

Table 1 Signal State of Receiver and Controller Ports

Input Signal Number	State of Ports Code of Signal P2.4～P2.0	(Hex)	Output Signal of Controller PulseWidth (ms)	Duty Cycle (%)
01	1 1110	0X1E	100	80
02	1 1100	0X1C	100	70
03	1 1101	0X1D	100	60
04	1 1001	0X19	100	50
05	1 1011	0X1B	100	0
06	1 0011	0X13	100	70
07	1 0111	0X17	100	80
08	0 0111	0X07	100	90
09	0 1111	0X0F	100	100
10	Others	0	0	

4.1 Software Control Flow

Figure 9 is the flow chart of software control of the controller. The controller begins to work upon power-on, and the circuit begins to check whether the position signal sent from the receiver is effective or not (no input is regarded as ineffective). When the signal is effective, the controller judges whether the working mode at the moment is automatic or manual. If it is the manual mode, the artificial direct intervention in the output of hydraulic controlling signals is allowed; if it is the automatic mode, the controller disposes the input effective signals, outputting controlling signals to the hydraulic system and driving signals to the pilot lamps.

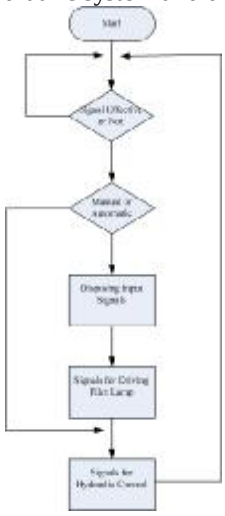


Figure 7 Software-Control Flow Chart of Controller

5. Controller VHDL Software Module Design

5.1 UART Module Design

Basic UART communication only needs two wires to transfer information; one is the RXD signal wire, and the other TXD wire. Its working mode can be full-duplex mode. TXD is the sending end of UART, outputting signals; RXD is the receiving end, inputting signals. The basic principle of UART is shown in Figure 8:

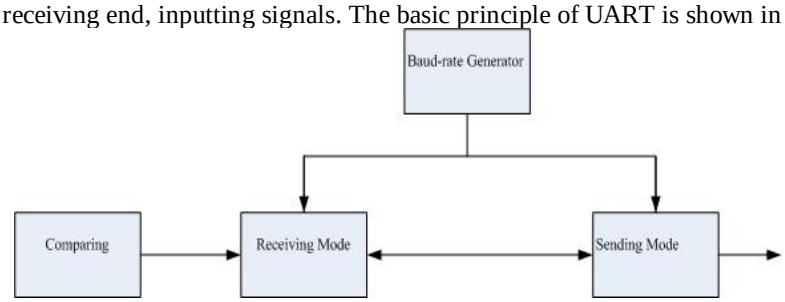


Figure 8 Basic Principle Diagram of UART

Through the schematic diagram, we can see that UART is mainly composed of four parts: baud-rate generator, sending module, receiving module and comparing module. The baud-rate generator generates a local clock signal that is higher than the baud rate, sampling RXD constantly, making the receiver and the controller keep pace with each other. The receiving module of UART receives the serial signals from RXD and transforms them into parallel data. The sending module transforms the parallel data to be output into TXD serial-output signals according to the basic frame format[17].

1. Baud-rate Generator Module

The baud-rate generator is actually a module that divides the frequency of the system clock. After frequency division, it outputs the clock signal of sampling RXD[18]. The clock frequency of the External Crystal Oscillator used for CPLD in this research is 3.6864MHZ, and the baud rate of asynchronous serial communication is 9600bit/S, so it needs to divide the frequency of the system clock to get a clock of 9600HZ. In order to improve the fault-tolerance disposal of the system, it requires the output clock of the baud-rate generator be N times of the baud rate of the actual serial data, and N can be 6、16、32、64. In this design, N is 16. Figure 9 is the logic diagram of baud-rate generator. Clkin is the clock-input end, and clkout is the clock-output end, outputting clock signals whose frequencies have been divided. Figure 10 is the schematic diagram of created RTL after synthesizing the VHDL codes of the baud-rate generator.

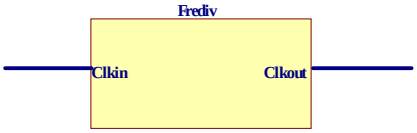


Figure 9 Logic Diagram of Baud-rate Generator

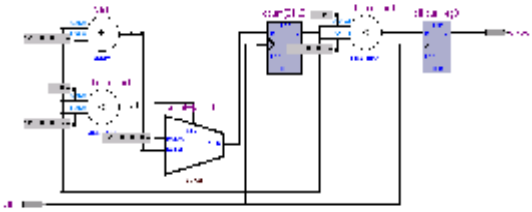


Figure 10 Synthesized Diagram of Baud-rate Generator

2. Asynchronous Receiving Module

The logic diagram of the asynchronous receiving module is shown in Figure 10. In the Figure, clk is the clock-input end; RX is the serial-data-receiving end; Sig1 is the sign of receiving interruption; After RX module has received one frame of data, Sig1 is loaded 1 automatically; q[7..0] are parallel-data-output end.

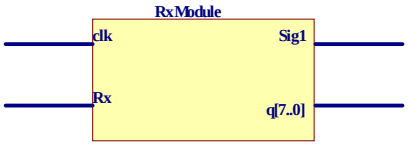


Figure 11 Logic Diagram of Synchronous Receiving Module

Figure 12 is the program flow chart of the asynchronous receiving module: sig1 is the sign of receiving interruption; when sig1 is in low electrical level, it indicates that the receiving process has not been started up, thus checking the electrical level of RX. When RX is in a low electrical level, sig2 begins to count; if RX is in low electrical level in consecutive 8 times of sampling, it indicates that this is the start bits, thus starting up the receiving process, receiving one bit of data every 16 receiving clock until it completes receiving all the 11 bits. The parallel-output end is a serial-to-parallel end, and the output data will change as the bits shift because it does not have the latch function[19].

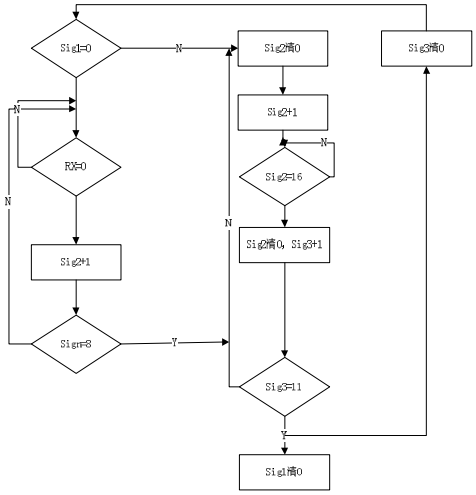


Figure 12 Flow Chart of Asynchronous Receiving Module

3. Asynchronous Sending Module

The logic diagram of the asynchronous sending module is shown in Figure 13. In the module of Tx Module, indata[7..0] are the 8-bit data-input end. CS is the chip-selection signal, which is effective in low electrical level. Wr is the output-permission, which is effective in high electrical level. Clk is the clock-input signal, providing clock signals for sending data. Txd is the serial-sending end for sending serial data. Ti is sending-interruption signal, which means sending when it is in high electrical level, and unused in low electrical level.

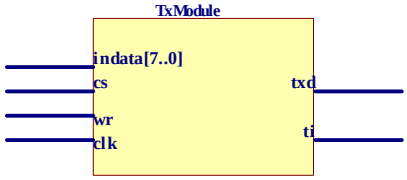


Figure 13 Logic Diagram of Asynchronous Sending Module

The program flow chart of this module is shown in Figure 14. When the rising edge of the clock signal comes, if CS is in low electrical level, it will check whether the signal written into wr is effective. If wr is effective, it indicates that the asynchronous sending module has data to be sent; if sig_buffer is 0, it means that the sending is not busy, and it can continue reading in data; if sig_buffer is 1, it indicates that the asynchronous serial-sending module is sending data right now, which is unable to respond to the order from the controller, and the control has to wait.

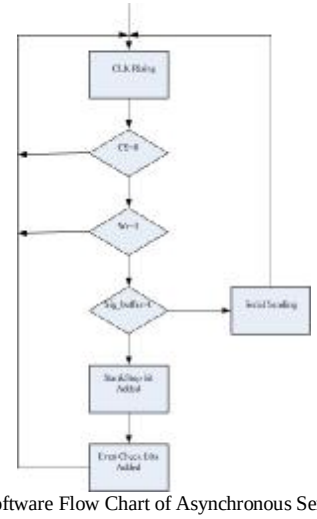


Figure 14 Software Flow Chart of Asynchronous Sending Module

5.2 Adjustable-Duty-Cycle of Hydraulic Controlling Signal Module

The adjustable-duty-cycle of hydraulic controlling signal module outputs PWM signals of different duty cycles mainly according to the different ground modes and different position signals chosen by users. Figure 15 is the logic diagram of this module. Sig[4..0] receive position signals from the receiver; Mode is the ground-mode-selecting-input end, and users can select hydraulic controlling signals of different duty cycles according to different conditions of ground work (paddy field or dry land). Clk is the clock-input end; Clkdown is the falling-signal-output end after frequency division, and ClkRaise is the rising-signal-output end after frequency division.

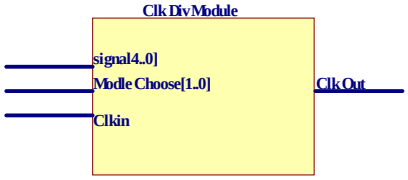


Figure 15 Logic Diagram of Adjustable-duty-cycle of Hydraulic Controlling Signal Module

Figure 16 is the RTL diagram after synthesizing the adjustable-duty-cycle of hydraulic controlling signal module, and the simulation diagram is shown in Figure 17. RTL is a created gate-level net list after translating the hardware description language (VHDL), and a crucial step in transforming the high-level description to hardware circuit. In the simulation diagram, sig[4..0] are the position-signal-input end; clk is the clock-signal-input end; Modle Chose is the mode-selecting-input end, and 1 means dry-land mode, 0 paddy-field mode. Clkdown and clkraise are hydraulic-controlling-signal-output end. From the simulation diagram, when mode=1 (dry-land mode) and the position signal is 11110 (high-level land), Clkdown outputs a falling-control signal with the duty-cycle of 60%. When mode=0 and the position signal is 01111 (low-level land), Clkraise outputs a rising-control signal with the duty-cycle of 100%.

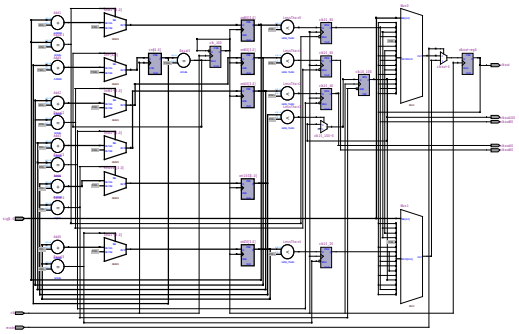


Figure 16 Adjustable-duty-cycle of Hydraulic Controlling Signal Module

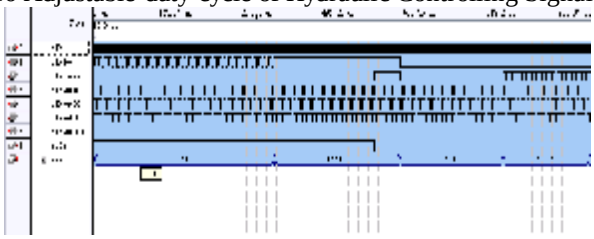


Figure 17 Sequential Simulation Diagram

5.3 Mode-selecting Circuit

The mode-selecting circuit is mainly used to judge whether to control the hydraulic system in automatic mode or in manual mode. The mode-selecting function of this circuit is achieved mainly through the CPLD software, and the function of manual intervention in the up and down of the ground shovel in the automatic mode is added, providing some convenience for users to operate according to the practical situation. Figure 18 is the RTL diagram of the logic-judgment module. There are 6 input signals in the circuit. Figure 19 is the sequential simulation diagram of this module.

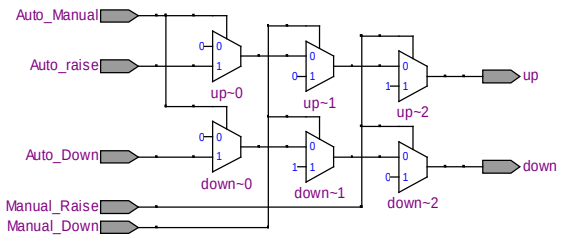


Figure 18 Integrated Result of Logical Judgment

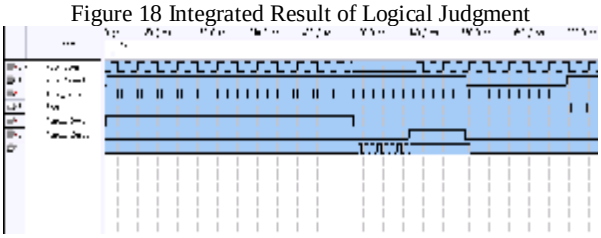


Figure 19 Sequential Simulation Diagram

6. Conclusion

This essay firstly introduces the overall design and the hardware structure design of the controller. Then it respectively aims at the controlling unit, the power convert module, the pilot-lamp-driving module, the hydraulic-driving module, the RS485 communication module, and makes some designs for these hardware circuits. Finally it tries some optimum designs for the software of the controller, using the hardware description language VHDL to carry out UART module, and developing the mode-selecting module and duty-cycle-adjusting module. The controller can choose proper hydraulic-controlling signals according to different landforms so as to fit in with both paddy field and dry land. The main results is:

1. CPLD was used as the logic control chip of this system. It enhances the system's ability to control. Its control capability is better than existing controller with MCU and its power consumption is further reduced.

2. The online changing ability of CPLD could enable quick update of the function of the controller, therefore makes it possible for the users to choose the most suitable software for the terrain, therefore maximize its efficiency.

3. Within CPLD, by programing with software, the interlock of automatic mode and manual mode is realized, therefore decreases the magnitude of the circuit and increases its stability.

4. Transmission by RS-485 can bus increases the stability and reliability of the working process.

7. Acknowledgement

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