THE HARDWARE RESEARCH OF DUAL-PORT RAM FOR MAIN-SPARE CPU IN RURAL POWER TERMINAL SYSTEM OF POWER QUANTITY COLLECTION

Ping Yang [1] , Shu Dai [2] , Xiuhua Wu [1] , Yong Yang [1,*]

[1] *College of Information and Electrical Engineering, Shenyang Agricultural University, Shenyang, China, 110161;*

[2] *Anshan Electricity Power Bureau, Anshan, China, 114001*

* *Corresponding author, Address: College of Information and Electrical Engineering, Shenyang Agricultural University, 120 Dongling Road, Shenyang, Liaoning, 110161, P. R. China, Tel:+86-24-88487860, Fax:+86-24-88487122, Email:xdxy7128@126.com*

Abstract: With the development of rural power market in our country, how to improve the operation more correctly and timely of power quantity collection, transmission and processing becomes a problem. The requirement of equipment in power quantity collection needs new and higher demands. The advantage of using dual-port RAM and main-spare CPU structure, when main CPU running, spare CPU supply monitoring of main CPU status messages, once main CPU break down, spare CPU could instead of main CPU completely. This paper introduces collectivity design in flow chart, hardware design include theory and application in detail. Using dual-port RAM to communicate between the main and spare CPU not only make sure the transmission efficiency, good anti-jamming performance, improve the speed of disposal, but also reduce the costs, making the operation of rural power network more security, economy and reliability. In rural power terminal system of power quantity collection has broad application prospects.

Keywords: dual-port RAM, main-spare CPU, terminal of power quantity collection, parallel communication, data exchange.

1. INTRODUCTION

To meet he need of power industry change into commercial operation has many requirements, how to improve power quantity collection, transmission, accuracy, reliability and operation in time are all the factors to be considered. With the development of Chinese power industry market, electric power department has already adopted power quantity as standard for expense, test, rewards and punishment. Therefore, higher requests are required on device of power quantity collection. Building a power quantity management system that based on automation is imperative under the situation.

Terminal system of power quantity collection provides multi-route data collection, information storage, inspect, check, balance calculate, prevent analysis of steal electricity, analysis of degradation loss, assess and so on, the most important thing is reliability. Therefore adopt one CPU will have some risks, once CPU has some problems, the data should be lost. If adopt two systems that supply for each other, need two powers, machine interfaces and so on. In this way the cost should be higher. Therefore, this system adopts the structure of main-spare CPU; both of them adopt the chip of ARM that has high performance (Chen et al., 2005). When main CPU running, spare CPU supply monitoring of main CPU's status, once the main CPU appears the problem, the spare CPU can instead the main CPU to carry on the work completely. Moreover, using dual-port RAM to communicate between the main and spare CPU not only make sure the transmission available, improve the speed of disposal, but also good at anti-jamming, making the operation of electric power system more security (Jia et al., 2006).

2. THE MAIN DESIGN PLANNING OF SYSTEM

The main-spare CPU is different from the master-slave CPU. If the system adopt the master-slave of CPU, the relationship of master CPU and slave CPU are leader and subordination, which means master CPU and slave CPU can be seen one CPU to carry out all the functions, just burden the different work in the system (Huang et al., 2004).

This terminal system adopts the structure of the forward plug-in type, each plug-in passes communicates using panel bus, and display and keyboard link the CPU through the cable, this system contains 5 plug-in parts, including copy meter panel, pulse panel, remote control panel, remote supervision panel and CPU panel (Ti et al., 1999). This design of plug-in provides the convenience to the install and debug for spot, any plug-in passes have no differences and can insert any module, but its address are different and each slot contains an unique address, thus any module has its own address after inserting the slot, this method can eradicate stir the wrong address completely (Liu et al., 2006).

The system adopts main-spare CPU, there are isolated in the functions, which means the two CPU can achieve the terminal's functions

independently. Therefore, the two CPU have their own connection, including broadcasting station, alternating equipment is interface between man and computer, other function panels (Jia et al., 2006). The configuration of the whole system is shown in figure1:

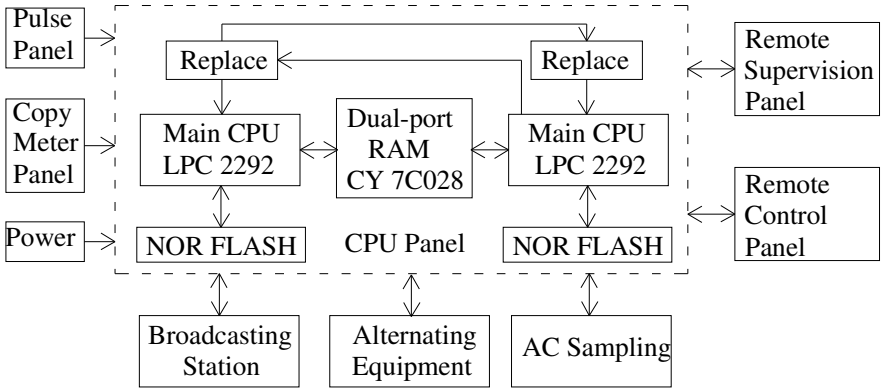

Figure1: System configuration chart

3. THE DESIGN OF HARDWARE

3.1 CPU panel

The dual-port RAM adopts CY7C028 of CYPRESS corporation. It has 64K x 16 static RAM, the access speed is less than 25ns, it has a true dual-ported memory cells which allow simultaneous access of the same memory location, the both ends has the independent control signal bus, the address bus and data bus. The CY7C028V consist of I/O and address lines, and control signals (CE, OE, R/W) (Cypress Semiconductor Corporation, 2002). These control pins permit independent access for read or write to any location in memory.

Program memory adopt SST39VF160 as NOR FLASH, it is CMOS multi-function FLASH (MPF) machine piece of the SST corporation, the memory capacity is 2MB, 16 bit data width, work voltage is 2.7V-3.6V. NOR FLASH have the same interface as SRAM which provide enough address to lead the pin to seek address, which can access each byte in chip easily and address lines and data lines of the NOR flash are divided, thus the efficiency of transmission is very high and the performance can be implemented in the chip.

3.2 Copy meter panel

Copy meter module adopts ST16C552 and extend RS-485 interface with two photoelectric isolations as the communications to meter. Each RS-485 interface can connect 32 blocks electricity meter with RS-485 interface (Mladen et al., 2001).

3.3 Remote supervision pulse panel

Remote supervision and pulse interface are consisted of import transform circuit, photoelectric isolation circuit, sampling circuit. Electromagnetism disturb of import signal is absorbed by pressure-sensitive resistor, after RC filter, then it enter photoelectric isolation circuit, last sampling is sent to XA-S30.The eliminate buffeting of signal is operated by software (Wang et al., 2004).

3.4 AC sampling unit

AC sampling circuit adopts ADS7864 that controlled by main CPU. AC sampling unit consists of voltage PT, current CT, corresponding analog signals disposal circuit and sampling A/D circuit. Main control panel can achieve all controls of circuit and data collection.

3.5 Broadcasting station

Broadcasting station adopts data transmission radio station. The customer can choose to use MODEM, fiber, GSM, GPRS or other communication methods. This broadcasting station is the vehicle radio stations with 200MHZ which made by New Zealand, it can place 16 pairs frequency of receive, dispatch and different blast-off powers, it also has call function, having the characteristics of channel establishment in a short time and high reliability (Deng et al., 2005).

4. IMPLEMENTATION OF DUAL-CPU FOR PARALLEL COMMUNICATION

Because this system adopts the structure of main-spare CPU, therefore the interfaces of data exchange become important parts that affect the whole system data processing ability. The whole hardware circuit connection is showed in figure 2.

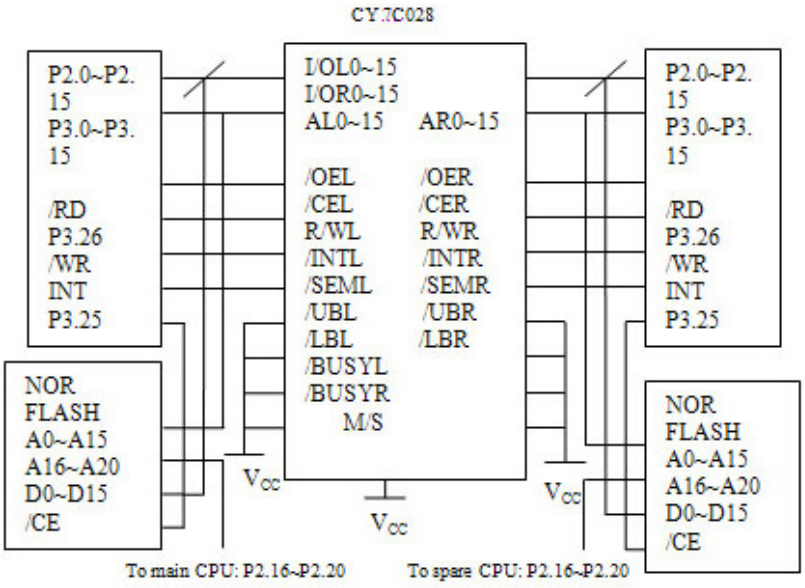

Figure 2: Hardware circuit connection chart

4.1 Data exchange

Using dual-port RAM achieve parallel communication between main-spare CPU means to share memory, which can lead data conflict, how to solve one memory for two sides to use together is the key point. CY7C028 has many solution modes, including hardware logic, interrupt logic, and semaphore logic (Cypress Semiconductor Corporation, 2004). According to the request of this system, when the main-spare CPU switching, need a great deal of data to communicate, and the data exchange is concentrated, therefore this system adopts the interrupt logic mode.

The interruption function of the CY 7C028 chip is use “mailbox” to achieve. For the hardware only need to link between the $/INT_R$ and $/INT_L$ of CY 7C028 and the main CPU and spare CPU respectively (Li, 1999). For the software only needs to write operation program and the interruption program.

4.2 Switching between main CPU and spare CPU

Here is discussing how to implement switching from the main CPU to the spare. Firstly, need to think about how to judge whether the work of main CPU is normal or not. Malfunction information of the main CPU can be

exchanged by dual-port RAM. The main CPU will accumulate data to the 0xE000 element regularly when the main program working that is the region of malfunction information in dual-port RAM. Then the spare CPU read Data_a from this element regularly and compared with the Data_b that is read before (Ji et al., 2004; Li, 2001). If the result D-value minus between Data_a and Data_b is constant which as same as schedule in advance, the program should be judged working normal; if the D-value is not the one, the main CPU must be in trouble. At this time, the spare CPU can compel the main CPU to reset. If no effecting, the main CPU can be judged have error or breakdown. Then the system changes into main-spare switching program.

After the spare CPU make sure the main CPU can not fulfill the task, it will take over the whole work of the main CPU automatically and write the main computer sign (main FLAG) to main-spare switching sign region 0xF001. When the main CPU resume normal, it must read the main-spare switching sign region 0xF001 first, if it's read main FLAG, then main CPU automatically change into spare CPU and write spare computer sign (standby FLAG) to 0xF000. At the same time, spare computer report terminal information to the main platform, the trouble is got away timely (Tang et al., 2001; Wang et al., 2005).

Nevertheless, with the development of electronic technology, the mass appear of 32-bit CPU provides conditions for main-spare CPU system. At beginning, because of processing speed of chip accelerating increasingly, only one chip can achieve the functions of system perfectly; moreover, with the chip price reducing, the cost of main-spare CPU system is lower (State Economic and Trade Commission, 2001). Main-spare CPU in a system, but independence with each other, can fulfill the task of system independently. That is say the main CPU in function is equal to the spare one. When the main CPU is in trouble and cannot resume back independently, after judgment system can switch main CPU to the spare one automatically. Then spare CPU can take over all work of main CPU that can prevent system's breakdown from main CPU's problems. In terminal system of rural power quantity collection, this structure can prevent loss of mass instant data from emerging issues of problem CPU and can reduce the cost of the whole system.

5. CONCLUSIONS AND FUTURE WORKS

Using high speed dual-port RAM and main-spare CPU structure to deal with the information, not only in the share data in the parallel network, make sure the information can easy get across the channel, improve the speed of transmission, be good at anti-jamming, but also with the price of lower-end

processor reducing, the cost of using main-spare CPU also can be decreased, in order to get more benefit in economy of rural power network.

The dual-port RAM and one-way store are the same in data store ability, simple interface, convenient operation, easy for communication, the communication processing and protocol in the two sides CPU are easily, only need to make sure the store space of data, the two sides CPU operate this space independently, in this way, the whole system can achieve high speed and reliability in the parallel communication. Otherwise, the dual-port RAM has good expansibility and easy for bit and byte expand, make sure the update operation for the future. Therefore, compared with the traditional double CPU communication, dual-port RAM has more superiority in main-spare parallel communication. Based on the dual-port RAM embedded multi-CPU system has good broad prospects in application of rural power enterprises.

To be worthy, when the designing of hardware and software, the distributed of store space, security issues of access in memory, failure handling, recovery and data redundancy should still be considered in detail of this main-spare CPU system, and also need to do some deeper research in the future.

ACKNOWLEDGEMENTS

As with any effort for this paper, there are a number of people who contributed to this in a roundabout way. Without their help, this paper would not exist.

Special thanks to professor Yang Yong, who is my PhD supervisor not only suggested the whole structure of design, but who always gave me good idea, no matter how odd.

Particular thanks are due to Dai Shu, the engineer of the Anshan electricity power bureau for sharing her knowledge and skills environment. The author is also grateful to associate professor Wu Xiuhua for her help, advice, comments, and excellent proofreading skills and gently showed me the errors in my ways.

Finally, the authors would like to thank the countless people who contributed to this paper with informal reviews and suggestions.

REFERENCES

Chen Deming, Xiong Liebin, Application of Dual RAM in Automation System, International Electronic Elements, 2005,No.4, pp.20-23.

Cypress Semiconductor Corporation, Interfacing the CY7C028V with Motorola's MPC860 Power QUICCTM Processor, 2002.

Cypress Semiconductor Corporation, 3.3V 64K×16 Dual Port Static RAM CY7C028V Data Sheet, 2004.

Deng Xiaogang, Xu Shiming, Tang Houjun, New Type of Power Amount Acquisition Terminal Based on Insert-style System, North China Electric Power, 2005, No.11,pp.42-45.

Huang Bin, Hu Rongqiang, Meng Qinghong, Design and Implementation of Real-Time Supervisory System Based on Dual CPU, Journal of WUT (Information & Management Engineering), 2004, Vol.26, No.2, pp.45-48.

Ji Qiang, Liu Liqiang, Application of Dual-port RAM to Data-acquisition System, Applied Science and Technology, 2004, Vol.31, No.5, pp.22-24.

Jia Guixi, Qi Le, Design of Data Supervision System Based on Dual CPU Structure, Engineering Science, 2006, No.4, pp.68-71.

Li Xiaoqing, The Application of Dual-Port RAM in the Computer Measurement and Control System of Multi-cpu, Control & Automation, Vo.15, No.1, 1999, pp.54-56.

Li Yufeng, Design of Two Monolithic Computers Parallel Communication System Based on Dual-port RAM, J.Changchun Inst.Tech. (Nat.Sci.Edi.), 2001, Vol.2, No.3,pp.56-58.

Liu Xin, Yin Zhiqiang, Mu Guobao, Ma Shidian, Research on Parallel Communication Based on Dual-port RAM in the Noncompetitive Pattern, Journal of Hefei University of Technology, 2006, Vol.29, No.2, pp.234-237.

Mladen Kezunovic,Yuan Liao. A New Method for Classification and Characterization of Voltages Sags. Electric Power Systems Research, 2001,Vol.58,No.1, pp.27-35.

National Instrument, A New Open Specification for Modular Instrumentation, 1997.

National Instrument, The PXI System Architecture, 1997.

State Economic and Trade Commission, Terminal System of Electrical Energy Collecting for Electric Power Industry, China Electric Power Press, 2001.

Ti Zhaoxu, Li Yuan, Design and Optimization Study of MIS of A Large Power Supply Bureau Client/Server System Being Used Successfully in Guangzhou Power Supply Bureau, Proceedings of the CSEE, 1999,Vol.19,No.5, pp. 85-88.

Tang lei, Zhang Boming, Sun hongbin, A Processing Method of Real-time Data in Energy Management System, Power System Technology, 2001,No.5,pp.15-19.

Wang Jing, Ji Xinsheng, Zhu Yunzhi, Strategies of Improving the High Usability of Application Software on Embedded OS, Control&Automation,Vol.21, No.82, 2005, pp.42-44.

Wang Junliang, Yuan Yijiang, Zhang Jiang, The Design and Application of Electric Energy Acquisition Terminal Based on GSM Communication, Journal of Henan Mechanical and Electrical Engineering College, Vol.12, No.2, 2004, pp.42-44.