A Floorplan-Based Power Network Analysis Methodology for System-on-chip Designs

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Abstract. In order to enable the single-pass design methodology, the planning of power distribution should be performed as early as possible. In this paper, we will tackle this problem at the floorplan stage. First, at the block level, we will present an effective method to model the behavior of local power network structure of a reused block. Next, at the full-chip level, we will present a floorplan-based power network analysis methodology for system-on-chip (SOC) designs. The proposed methodology works well because it uses suitable models to represent the local power networks of blocks according to the properties of blocks. Experimental data shows that the new modeling technique can identify the most critical drop voltage of a reused block and the floorplan-based analysis methodology is useful for the planning of power distribution network of a SOC design.

Keywords: Modeling, Voltage Drop, Power Consumption, and Reused Block.

1. Introduction

Power distribution is always very important in the design of VLSIs because power network covers a large portion of chip area. So it is given the first priority in routing process [1][2]. There are two basic problems in the design of power network. The first is the undesirable wear-out of metal wiring caused by electromigration, and the second is the narrowing margins causes by voltage drops. Increasing wire widths can solve these problems. But it is too expensive to use the wiring resources freely.

In the deep submicron technology, the metal width tends to decrease with the length increasing due to the complex system integration into single silicon. Therefore, the resistance along the power metal line increases. Chips that are under-designed with a smaller margin often fail on the test bench or later in the field. However, most of the commercially available tools focus on the transistor-level and post-layout verification of power distribution. If any problem related to electromigration or voltage drop is revealed at this stage, it is very difficult or expensive to fix. In order to enable the single-pass design methodology, the accurate planning of power distribution should be performed as early as possible. In this paper, we will present a floorplan-based power network analysis methodology for system-on-chip (SOC) designs.

At the floorplan stage, the chip area is divided into a set of non-overlapping physical blocks by power trunks. Each physical block consists of many rows. Cells are placed on the row so that the power is fed from the power rail. The two end points of a power rail are the power trunks. Because of consistency between cell library and power rail, and wiring resource economy, the line width of power rail may not be increased. In other words, the local power network structure in a physical block is often fixed. However, with the increase of chip size, power supply current for more than a hundred cells is to be fed through this thin rail. The power trunks are necessarily used to improve the reliability and quality of power distribution. Therefore, the design and analysis of power network is important for SOC designs.

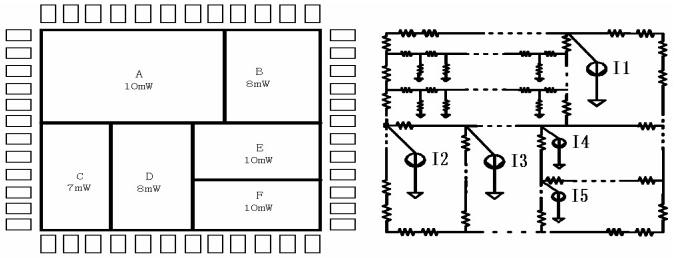
The main distinctions of our work are elaborated as the below:

- At the block level, we will propose an effective method to model the local power network structure of a reused block, whose power consumption was already measured by real instruments. As a result, when we integrate the reused block into a SOC design an accurate equivalent resistive circuit can be used to describe the behavior of local power network structure.
- At the full-chip level, we will propose an effective methodology to analyze the power distribution of a SOC design. As a result, the designer can accurately predict the electromigration or voltage drop problem at the floorplan stage. If any reliability problem is found, the designer can make power network changes when they are easiest and least costly to implement.

The rest of the paper is organized as the below. Section 2 briefly introduces the problem and surveys the related works. In Section 3, we will present a new modeling method, which is well suitable to model the behavior of local power network structure of a reused block. Next, a floorplan-based full-chip power network analysis methodology will be proposed in Section 4. Some experimental results will be reported in Section 5. Finally, we will give some concluding remarks in Section 6.

2. Preliminaries

At the stage of floorplan, the power trunks form a global power network and divide the full-chip into several blocks. Let's use Figure 1 as an example. Figure 1 (a) is a floorplan, whose blocks are divided by global power network. Figure 1 (b) illustrates an equivalent circuit of its power distribution.



(a) (b)

Figure 1: (a) A floorplan. (b) An example of equivalent circuit of its power network.

At the block level, where local hot spots are located, a finer grid will be generated to model the local power network structure. The power grids may be defined as below. Each physical block consists of many rows. On each row, the power rails of adjacent cells are connected together. A straightforward method is that each cell in the row is represented as a grid.

Most previous works use the equivalent current source model [3][4] to describe the local power network structure of a block at the floorplan stage. The assumptions of the equivalent current source model are elaborated as below.

- All the switching activities within one block are lumped together.
- The current sources are uniformly distributed at the grids.

The equivalent current source model is useful for modeling blocks at floorplan view, where placement and route have not been done. The basic technique of equivalent current source model is described as the below. Suppose that the power consumption of a block, which is usually reported by the dynamic gate-level power calculator, equals to P_{block}. Note that, in order to tackle the worst case, P_{block} is usually the peak power consumption. Then, for this block, the equivalent current source Iblock is equivalent to P_{block}/V_{DD}. Assumes that this block consists of m rows and each row has n grids. Thus, for each gird in this block, the equivalent current source Igrid is Iblock/(m*n). As a result, for each grid in this block, the resistance Rgrid equals to VDD/Igrid. The Rp is equivalent to Rs * row length / power rail width, where Rs is unit resistor. The method to calculate Rring is similar to RP.

3. The Modeling Technique for Reused Blocks

In this section, we will present an effective modeling technique for the local power network structure of a reused block, whose power consumption was already measured by real instruments. Our motivation is shown in Section 3.1. Then, our method is given in Section 3.2.

3.1 The Motivation

First, we borrow the material from [5] to describe the equivalent current source modeling technique as below. In the equivalent current source modeling technique, the value of equivalent current source is obtained without considering the resistances in the power rails. As a result, when the metal resistances in the power rails are added into the equivalent circuit, the power consumption will be varied. In other words, the power consumption of the equivalent resistive circuit derived by this model will be different from the original given power consumption.

Let's use the unit placement row shown in Figure 2 as an example. A unit placement row is a resistive network whose end points are power trunks. The unit placement row in Figure 2 consists of the resistors R_{P1}, R_{P2}, R_{P3}, R_{P4}, R_{P5}, R_{C1}, R_{C2}, R_{C3}, and R_{C4}. The values of R_{P1}, R_{P2}, R_{P3}, R_{P4}, and R_{P5} are extracted from technology parameters. Assume that P_{row} is the given power consumption of the unit placement row. Then, if using the equivalent current source model, the values of R_{C1}, R_{C2}, R_{C3}, and R_{C4} are obtained by the following equation:

$Rci = (4*V_{DD}^2)/P_{row}$, where i=1,2,3,4

Let P_{RP1}, P_{RP2}, P_{RP3}, P_{RP4} and P_{RP5} be the power dissipation of resistors R_{P1}, R_{P2}, R_{P3}, R_{P4}, and R_{P5} respectively. From [5], the power consumptions P_{RP1}, P_{RP2}, P_{RP3}, P_{RP4} and P_{RP5} can be calculated as follows.

$P_{RP1} = (V_{S1} – V_{M1})2 / R_{P1}$

$P_{RP2} = (V_{M1} – V_{M2})2 / R_{P2}$

$P_{RP3} = (V_{M2} – V_{M3})2 / R_{P3}$

$P_{RP4} = (V_{M3} – V_{M4})2 / R_{P4}$

$P_{RP5} = (V_{M4} - V_{S2})2 / R_{P5}$

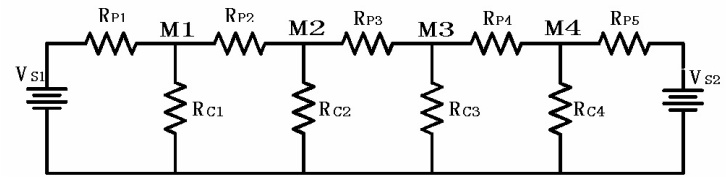


Figure 2: An example of unit placement row.

Let P_{RC1}, P_{RC2}, P_{RC3} and P_{RC4} be the power dissipation of resistors R_{C1}, R_{C2}, R_{C3}, and R_{C4} respectively. The power consumptions P_{RC1}, P_{RC2}, P_{RC3} and P_{RC4} can be calculated as follows.

$P_{RC1} = V_{M1}^2 / R_{C1}$

$P_{RC2} = V_{M2}^2 / R_{C2}$

$P_{RC3} = V_{M3}^2 / R_{C3}$

$PRC4 = V_{M4}^2 / R_{C4}$

Therefore, the total power consumption P_{total} of this resistive network is given by the following equation:

$P_{total} = P_{RP1} + P_{RP2} + P_{RP3} + P_{RP4} + P_{RP5} + P_{RC1} + P_{RC2} + P_{RC3} + P_{RC4}$.

It is obvious that P_{total} is not the same as P_{row}, which is the original given power consumption. In other words, although we use P_{row} to obtain the equivalent current source, the power consumption of the derived resistive circuit is not equivalent to P_{row}. However, the P_{row} may also often be over-estimated, because dynamic gate-level power calculator does not tackle metal resistances. Therefore, although there is a difference between P_{row} and P_{total}, the equivalent current source model still works well in specifying the power grid requirements for typical ASIC design flow.

However, due to the trend of SOC design methodology, a block may be reused from a previous production chip. In such case, real instruments can measure the power consumption of this reused block. Once a block is measured, we need to be able to reuse the accurate measured result, rather than having to re-estimate for the block. Therefore, it is desirable to have a power network modeling technique such that the P_{total} equals to P_{row}. To achieve the goal, we need to have a different method to model the behavior of local power network structure.

3.2 The Proposed Method

The problem we study is described as the below. Given a measured power consumption of a reused block, find the value of equivalent grid resistance such that the power consumption of the derived resistive circuit is identical. With the same assumption as [3][4], we suppose that all grid resistances are the same. Let's use Figure 2 as an example. Suppose the reused block has m rows and the measured power consumption is P_{block}. Then, the P_{row} is P_{block}/m. The values of R_{P1}, R_{P2}, R_{P3}, R_{P4}, and R_{P5} can be extracted from technology parameters. Thus, our problem is to find the value of grid resistance RC such that $R_C = R_{C1} = R_{C2} = R_{C3} = R_{C4}$ and $P_{row} = P_{total}$.

It is difficult to find the correct R_C directly. Our method is to iteratively solve the linear resistive network and calculate the P_{total} in each time of iteration. The initial

value of R_C is the same as the equivalent current source model. In other words, initially, $R_C = (n*V_{DD}^2)/P_{row}$, where n is the number of grids in a row.

```
Procedure Find_Grid_Resistance();
begin
R_C = (n*V_DD^2)/P_row;
solve the resistive network based on R_C;
while (|P_row-P_total|>tolerance) do
   begin
      if (P_row>P_total)
   then decrease R_C;
   else increase R_C;
   solve the resistive network based on R_C;
   end
end.
```

Figure 3: The algorithm to find the grid resistance R_C.

Note that the P_{total} is calculated in each time when the linear resistive network is solved. If P_{total} is smaller than P_{row}, R_C is decreased by a small value in the next time. If P_{total} is greater than P_{row}, R_C is increased by a small value in the next time. The iterations repeat until the difference between P_{row} and P_{total} are confined within a tolerance value. As a result, the value of R_C will be converged. The pseudo code of our method is given in Figure 3.

4. The Full-Chip Analysis Methodology

A SOC design often contains several blocks. In this section, we will present a floorplan-based full-chip power network analysis methodology, which is applicable to the design flow of a SOC design.

4. 1 Full-Chip Equivalent Resistive Circuit

The first step is to generate an equivalent resistive circuit to represent the full-chip power distribution. The algorithm is depicted in Figure 3. For the need of further analysis, the output is in SPICE format. The details of the algorithm are as below.

The algorithm translates all the power pads, power trunks, all the physical blocks into corresponding equivalent circuits, respectively. Firstly, the power pads are tackled. For each power pad, the supplied voltage value is set on its corresponding grid position. Then, for each power trunk, it is translated into a series of resistance Rtrunk, where Rtrunk is obtained as below:

(1) For a vertical power trunk, R_{trunk} = Rs * cell height / power trunk width.

(2) For a horizontal power trunk, R_{trunk} = Rs * cell width / power trunk width.

Next, the local power network of each physical block is translated into equivalent resistive circuit according to the property of this block. For the blocks, whose power

consumptions are reported by dynamic gate-level power simulator, their local power networks are generated into SPICE netlist using equivalent current source model. For the blocks, whose power consumptions are measured by real instruments, their local power networks are generated into SPICE netlist using the model presented in Section 3.2.

```
Procedure Generate_Full_Chip_Netlist();
begin
for each power pad do
  set the voltage value on the corresponding grid;
for each power trunk do
 generate the corresponding resistive circuit;
for each physical block do
   begin
    if it is a reused block
     then
        generate the corresponding resistive circuit using the model as shown in
            Section 3.2;
     else
        generate the corresponding resistive circuit using the equivalent current
            source model;
  end
end.
```

Figure 4: The algorithm to generate an equivalent resistive circuit for the full-chip.

Finally, all the equivalent circuits, including power pads, power trunks, and physical blocks, are combined together. As a result, a full-chip equivalent resistive circuit in SPICE format is already generated.

4.2 The Analysis Procedures

After the full-chip equivalent resistive circuit is obtained, we can perform full-chip power network analysis through SPICE simulation. Because of metal resistances, the full-chip simulation has the following properties:

- The voltages on different grids of the global power network are different.
- The voltages on different grids of a block are different.
- For the same grid in a block, the voltage will be varied when the block is integrated into a SOC design.

Even though a block is safe in the block level analysis, it still may have voltage drop or electromigration problem in the full-chip analysis.

Early analysis enables us to make power network changes when they are easiest and least costly to implement. Because of consistency between cell library and power rail, the values of Rc and Rp in a block are often fixed. Therefore, if any voltage drop or current density problem found in the full-chip power analysis, the designer need to widen the power trunks or add more power trunks. Whenever the global power

network is modified, the voltages on power grids may be varied. The effects caused by the modification of global power network are summarized as the below:

- The voltages on the grids of the global power network will be varied, because the corresponding resistances (i.e., Rtrunk) are increased or decreased.
- The voltages on the grids of a row will be varied, if any one voltage at the end points is varied.

If the power network is modified, a new equivalent resistive circuit is generated. Then, the modified power network should be validated again through SPICE simulation. The procedure repeats until no reliability problem found in the final power network.

The analysis methodology can be further generalized. Suppose that a SOC design has M execution modes. Thus, M equivalent resistive circuits need validation. The procedures are elaborated as below. Assume that the SOC design contains N blocks, including B_1, B_2, …, and B_N. Let $P_i(B_j)$ be the peak power consumption of block Bj at execution mode i, where $1 \le i \le M$ and $1 \le j \le N$. For each $P_i(B_j)$, where $1 \le i \le M$ and $1 \le j \le N$, we can choose the suitable modeling technique to describe the local power network structure. Next, for each execution mode i, we can obtain the corresponding full-chip equivalent resistive circuit according to $P_i(B_j)$, where $1 \le j \le N$. As a result, we will have M full-chip equivalent resistive circuits. Note that all the M equivalent resistive circuits should be validated through SPICE simulation. If any reliability problem is found, the related power trunks in the global power network are modified. Based on the modification, new M equivalent resistive circuits are generated. The procedures repeat until no reliability problem can be found.

5. Experimental Results

We have developed the floorplan-based full-chip power network analysis algorithm by using C programming language and integrated it with Star-Hspice on a Sun UltraSPARC-10 workstation. In the following, we will report some experimental results to show the effectiveness of the proposed analysis methodology. The first experiment reports the experimental results on the new modeling technique and gives the comparisons with other approaches [3][4][5]. The second experiment reports the studies on the resolution of grids. In these experiments, four test cases, which resemble the unit placement row in a real block, are used to test the effectiveness of the proposed analysis methodology.

Table 1 tabulates the characteristics of these four test cases with the measured power consumption, the voltage on the end points, and the row length. Without loss generality, we assume the voltages on the two end points are the same. However, note that, due to the metal resistances in power trunks, the voltages on the two end points of a row are often different with each other.

Table 1: Summary of test cases.

Test Case	Measured Power	Voltage at End Points	Row Length
CKT1	8 mW	1.8 V	1500 µm
CKT2	4 mW	1.8 V	5000 µm
CKT3	25 mW	1.8 V	700 µm
CKT4	20 mW	1.8 V	250 µm

5.1 Studies on the New Modeling Technique

We compare the new modeling technique with previous works [3][4][5]. Table 2 tabulates the experimental results. The results include the comparison of (i) the derived equivalent grid resistance RC (the unit is in ohm); (ii) the power consumption of the derived equivalent resistive circuit; (iii) the minimum voltage found in the equivalent resistive circuit (the unit is in volt); and (iv) the CPU time to analyze the test case (the unit is in second).

As shown in Table 2, the equivalent resistive circuits derived from our approach have the same power consumption with the original given power consumption (i.e., the measured power shown in Table 1). On the other hand, the power consumptions of equivalent resistive circuits derived by other approaches are less than the original given power consumption. Moreover, because the metal resistances in the power rail are taken into account to derive the equivalent circuit, experimental data also shows that our approach can identify the most critical drop voltage.

Table 2: Experimental results on different modeling techniques.

Test Case	Method	Derived R_C	**Derived Power (mW)**	Minimum Voltage Found	CPU time (second)
CKT1	**Ours**	3751099	**8.0**	1.601	0.20
	[3][4]	4049999	7.4	1.614	0.10
	[5]	4049999	7.3	1.616	1.77
CKT2	**Ours**	7115399	**4.0**	1.474	0.26
	[3][4]	8099999	3.5	1.508	0.12
	[5]	7940414	3.6	1.504	1.77
CKT3	**Ours**	1157669	**24.9**	1.513	0.30
	[3][4]	1295999	22.5	1.540	0.12
	[5]	1295906	22.5	1.540	1.74
CKT4	**Ours**	1532480	**19.9**	1.654	0.24
	[3][4]	1620000	18.9	1.661	0.12
	[5]	1620000	18.5	1.665	1.80

The modeling technique of [5] is an extension of [3][4]. It repeats the procedures presented in Section 2 until a converged equivalent current source is obtained. As a result, the grid resistances obtained by [5] are different among all the grids in the row. The grid resistance of [5] reported in Table 2 is the minimum value.

5.2 Studies on the Resolution of Grids

At the block level, where local hot spots are located, finer grids are generated to model the local power network structure. The most comprehensive method is to define the resolution of grids as fine as possible. However, the CPU time may increase with the increase of the resolution of grids. Furthermore, the number of grids cannot be infinite. In order to study the effects caused by the resolution of grids, we analyze the test cases with different number of grids. Without loss of generality, the new modeling technique is applied. Table 3 tabulates the results on the four test cases.

For each test case, given a number of girds, Table 3 reports the value of derived Rp, the value of derived Rc, the minimum voltage found, and the position of the minimum voltage, respectively. Obviously, with the increase of resolution of grids, the derived Rp decreases and the derived Rc increases. However, experimental data shows that, in the range of 1000 to 20000 grids, the values of minimum voltage are converged to the same value. In other words, 1000 grids are enough to find the minimum voltage in these test cases. Furthermore, note that 1000 is not the lower bound in these test cases.

Based on the observation as shown in Table 3, we know that the critical drop voltage can be identified with a coarser resolution of grids. As a result, the CPU time of full-chip simulation can be significantly reduced.

6. Conclusions

In this paper, we presented an effective modeling technique for the local power network of a reused block. If compared with existing models, the main distinction of the proposed approach is that the power rails are into account to derive the equivalent resistive circuit. Experimental data shows that the proposed modeling technique can identify the critical drop voltage in reused blocks. We have developed a floorplan-based full-chip power distribution analysis system, which uses different models to represent the power networks of blocks according to their properties. As a result, the designer can accurately predict the electromigration or voltage drop problem at the floorplan stage and make power network changes when they are easiest and least costly to implement. This power network analysis system is well suitable for a SOC design.

Table 3: Experimental results on different number of grids.

Test Case	The Number of Grids	Derived R_P	Derived R_C	Minimum Voltage	Position of Minimum Voltage
CKT1	**20000**	0.018213	7502199	**1.601**	749.6
	10000	0.036425	3751099	**1.601**	749.7
	8000	0.045530	3000899	**1.601**	749.7
	5000	0.072843	1875589	**1.601**	749.8
	2000	0.182052	750299	**1.601**	749.6
	1000	0.363922	374999	**1.601**	749.2
CKT2	**20000**	0.060711	14231308	**1.473**	2499.8
	10000	0.121416	7115399	**1.474**	2498.7
	8000	0.151767	5692299	**1.473**	2499.0
	5000	0.242809	3557599	**1.474**	2499.5
	2000	0.606839	1422969	**1.474**	2498.7
	1000	1.213073	711499	**1.473**	2497.5
CKT3	**20000**	0.008500	2315299	**1.513**	349.9
	10000	0.016998	1157669	**1.513**	349.8
	8000	0.021247	926099	**1.513**	349.9
	5000	0.033993	578899	**1.513**	349.9
	2000	0.084958	231499	**1.513**	349.8
	1000	0.169830	115719	**1.513**	349.6
CKT4	**20000**	0.024285	3064900	**1.654**	124.8
	10000	0.048567	1532480	**1.654**	124.8
	8000	0.060707	1225969	**1.654**	124.8
	5000	0.097123	766300	**1.654**	124.9
	2000	0.242736	306499	**1.654**	124.9
	1000	0.485229	153199	**1.654**	124.8

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