RISC/DSP Dual Core Wireless SoC Processor Focused on Multimedia Applications

Hyo-Joong Suh[1] and Jeongmin Kim[2]

[1] School of Computer Science and Information Engineering,
The Catholic University of Korea
San 43-1 Yeoggog 2 Dong, Wonmi Gu, Bucheon, Gyeonggido, 420-743 Korea
hjsuh@catholic.ac.kr
[2] GCT Semiconductor, Inc.
2121 Ringwood Avenue San Jose CA 95131

Abstract. The key technology of the mobile multimedia application is System-On-Chip processor that integrates the major function unit with low power consumption using a small battery. The wireless communication is practical technology, which makes comfortable communications between devices, such as IEEE 802.11a/b/g and Bluetooth. By the modern streaming technology with compression, like mpeg, the wireless communication triggers high quality media service without wires.
The wireless communication spend a quite large portion of energy of mobile device if data flows continuously, hence a delicate energy control may needed to fulfill a saving of the limited energy. Due to these issues, integrating the wireless function units into the high performance embedded processor supports a seamless control of power consumption of wireless part, and the communication data flows are sealed in the SoC chip, which reduces inter-chip communiaction energy between a main processor and a wireless media access controller.
We focused the high performance wireless multimedia applications are suffered by the energy consumption, so we alleviated the power issue by integrating of IEEE 802.11a/b/g media access controller, modem, ADC/DAC, high performance DSP, and RISC core in a silicon.
We present a wireless capable SoC processor, GDM5104, that integrated the multiple wireless media access controller as well as CCK/OFDM/GFSK modem and ADC/DAC also. Furthermore, the processor integrates RISC and DSP independent cores with appropriate caches, and rich peripherals that sufficient to implement mobile multimedia applications, hence the processor exhibits wireless connectivity with low power consumption. The processor is fabricated in a 0.18um standard CMOS technology, and operates at 133MHz RISC, and 100MHz DSP, which provides full capability of wireless multimedia processing.

1 Introduction

The progress of sub-micron technology allows an integration of various function units on a single system-on-chip (SoC), and appearances of some sophisticated

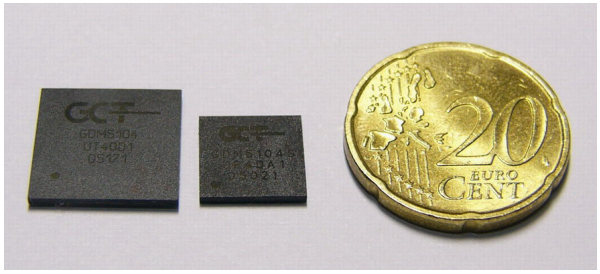

Fig. 1. GDM5104 embedded processor(256 pin, 169 pin fpBGA package)

multimedia processing algorithms induce a lot of multimedia applications that come onto the market. In terms of mobile applications, power energy is provided by primary or secondary batteries, which capacity is quite small to process a complex computation. Several energy saving methods are studied that include frequency control [1], voltage control [2], power control of peripheral block[3], and some power management techniques are implemented on the off-the-shelf embedded processors such as PXA270 by Intel[4].

Portability of a mobile application can be maximized if it communicates using wireless protocol. IEEE 802.11a/b/g [5] wireless standards are one of the rapidly imported technologies that applied on the mobile systems, however the wireless communications consume a lot of energy than wire communication standards such as USB and IEEE 1394. Hence the wireless mobile application is suffered by a shortage of energy, thus operation time is insufficient to play some multimedia titles.

Another issue arises from digital multimedia processing that consumes a lot of processor performance. Many multimedia processing algorithms are inefficient if it operates on the common reduced instruction set computer (RISC) style microprocessor, and if the multimedia algorithm processed on the RISC processor, it consumes lots of energy than a special unit for processing of the algorithm. By the viewpoint of energy consumption and performance, digital signal processing (DSP) processor is suitable to process a most multimedia algorithms, while the RISC processor performs better a general portion of the application code like user interface and TCP/IP protocol [6]. One example of the voice over wireless LAN that utilizes the wireless technology on mobile handset using voice over internet protocol. In this case, DSP processor supports to process speech vocoder, line/acoustic echo cancellation, DTMF, and CPT also. Parallel with the DSP processor, RISC processor supports the operating system, TCP/UDP/IP, RTP, device control, and other user interface parts.

By integrating of IEEE802.11a/b/g, RISC processor, DSP processor, USB2.0, NAND flash, IEEE802.3 MII interface, ATA, Bluetooth [7], and other peripherals on a chip, GDM5104, which presents a capability of powerful and energy-efficient operation in case of wireless mobile applications.

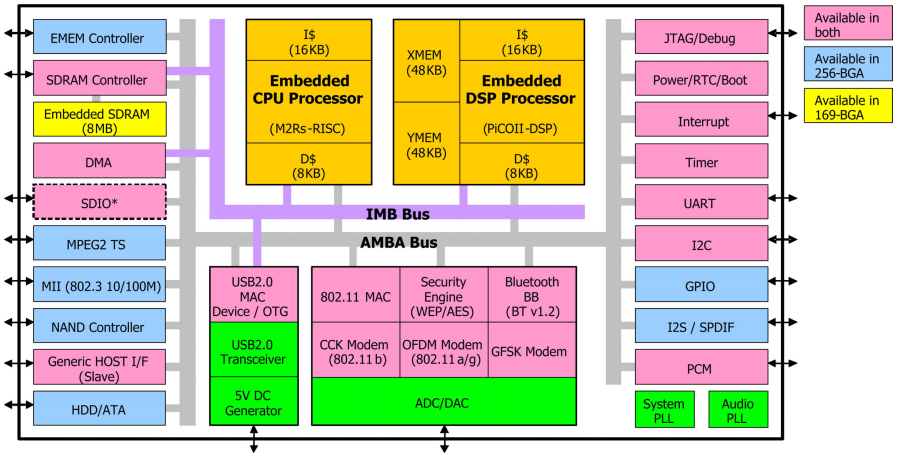

Fig. 2. Internal blocks of GDM5104 processor

Next section presents the detailed processor internals of chip and low power features. Section 3 describes operating system, software environment, and debug interface of the processor, and Section 4 shows early-stage performance evaluation. Finally, concluding remarks appear in Section 5.

2 GDM5104 Embedded Processor

The GDM5104 is a successor of GDM5302 [8], and these processors are wireless multimedia chips, which are under development. The advanced points of GDM5104 compared to the prior processor are independent structure of RISC and DSP dual processor cores and integration of wireless MAC/modem. Core of the prior GDM5302 processor was RISC/DSP hybrid structure that the core operates DSP mode or RISC mode exclusively, while the successor, GDM5104, has independent cores with independent caches respectively.

Figure 2 shows the dual cores and connected peripherals that exhibit lots of wireless and wire connectivity standards. Internal memory bus (IMB) is the high bandwidth internal bus that connects two cores and high-speed SDRAM, USB2.0, and DMA unit. Peripherals, DMA, and processor cores are connected via AMBA open standard bus [9] with enhanced features. There are two AHB buses of internal and external and APB bus for register access of peripherals. Each peripheral has two AHB bus masters for both AHB buses and one APB slave that will be used to access internal registers or command mapped coprocessor memory. XMEM (X-memory) and YMEM (Y-memory) are AHB slaves to internal AHB, and external memories are AHB slaves to external AHB. Therefore, internal AHB bus is used for the access between internal memories and AHB masters, and external AHB bus is used for the access between external memory and AHB masters. The enhanced features are multi-clock supporting and mul-

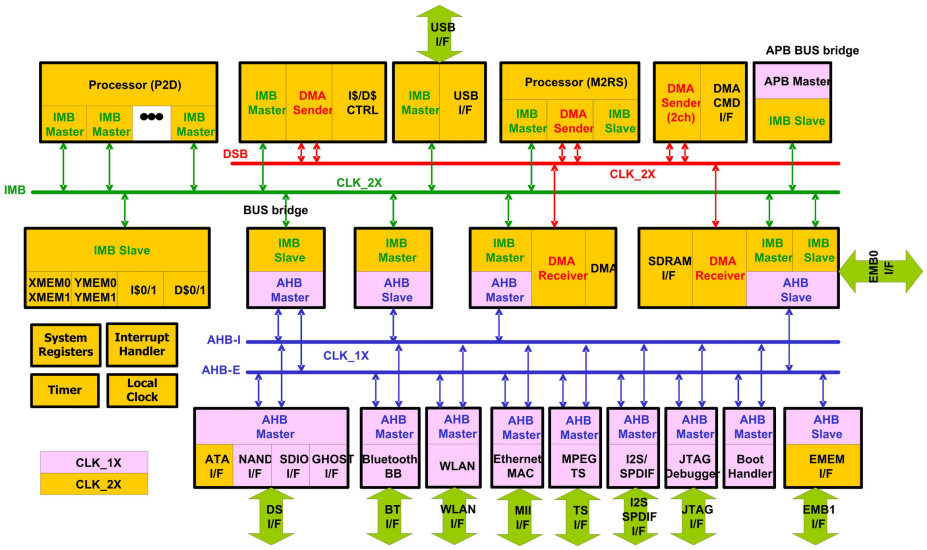

Fig. 3. System bus and operation clock of each block

tiple byte write operations which provides independent bandwidth control on each block to control an energy consumption of each block.

2.1 Internal bus architecture

Detailed bus architecture of the processor is shown in Figure 3. The memory access priorities of each masters are decided as round robin in AHB arbiter. Since external memory is only connected to external AHB bus, its access priority is dependent on the AHB arbiter. However, internal memory such as XMEM and YMEM is not only connected to internal AHB bus, but also connected to internal CPU and DMA directly. Memory accesses from internal AHB bus have highest priority than the lower priority accesses from processors and DMA requests. AHB and APB bus operates at 88 or 80 MHz fixed frequency while each block is connected to bus through interface logics that can operate by ratios of 44 or 40 MHz reference clock. Speed of function blocks are tuned by the requirement of the bandwidth, thus they operate using multiple or fixed frequency by application requirements.

2.2 DSP core

The architecture of the PiCOII-DSP (P2D) core is RISC/DSP hybrid structure that has the capable of processing of DSP instructions as well as RISC instructions also. The P2D was the main core of its precedence processor, GDM5302. Like other conventional RISC, P2D adopts fixed length instructions format for

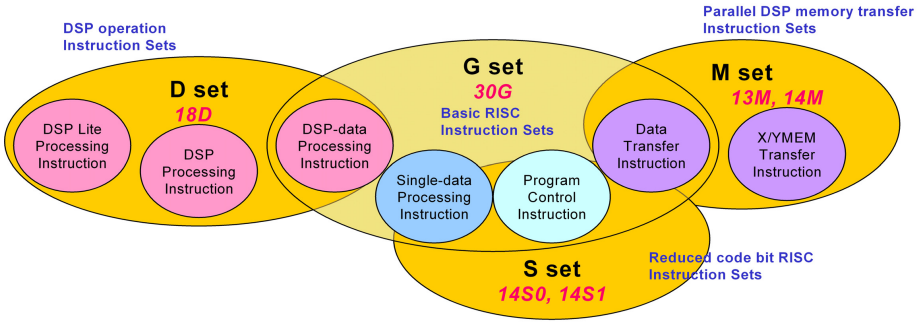

Fig. 4. Instruction sets classification of the P2D core

simple decoding, 32 general purpose registers, and load-store architecture. Furthermore, P2D supports additional features to support DSP application effectively, P2D adopts an extra datapath for MAC-base operations used in the conventional DSP. In addition to MAC-based datapath, P2D includes several DSP operations such as saturation, scaling and round operations [10] in the instruction sets. Also, it supports Single Instruction Multiple Data (SIMD) features, which results in high performance in 16-bit speech applications [11]. The shift amount field of the special DSP mode registers automatically scales the source or destination registers. In addition to the data cache, P2D employs the parallel memory access operations of the internal data memories such as XMEM or YMEM. Thus P2D provides high memory bandwidth requirements in real-time multimedia applications. For XMEM or YMEM accesses, P2D supports memory accesses with special registers for address calculation. With the special address mode registers, P2D supports various addressing modes used in the conventional DSPs such as circular and bit-reverse addressing, which are used in many DSP applications. The features of P2D can be summarized as follows.

- RISC and DSP operation, single G set issue, dual S set issues, dual M set issues, both D set and M set operation simultaneously
- 32bit fixed instruction set
- Five stage pipeline : FE - DE - E0 - E1 - E2
- Interrupt disable during instruction execution within delayed slot
- 4read-2write register file
- 16bit/32bit DSP operation with one 48bit accumulator and 4 address registers
- 24bit x 24bit signed multiplication
- SIMD operations
- 1 delay slot for decode stage branch and execution stage branch and link
- 2 delay slot for execution stage branch
- 1 delay slot for load operation

P2D core has RISC and DSP instruction sets by its hybrid architecture, the instructions can be classified by four sets. Figure 4 describes detail of instruction sets and classifications.

G set Basic RISC instruction set that including integer scalar and DSP data processing with single memory transfer and control handling. Encoded as 30bit width.

S set Compact encoded width which provides a subset of G instruction set with reduced opcode and register field. Encoded as 14bit width.

D set Fixed 16bit or 32bit DSP operation including accumulation. Encoded as 18bit width with extending register field.

M set Specialized for internal scratch-pad memory transfers with several addressing mode and address registers. Encoded as with 13 or 14bit width dependent on the size of register field.

2.3 RISC core

To optimize power consumption without sacrificing a performance that needed to operate a stream data manipulation with general network protocol and/or user interface processing, MiCROII-RISC (M2R) core is the embedded processor that used in mobile system that requires high-performance general operations along with the signal processing by the P2D. Instruction of the M2R core is the same as *G set* which is subset of the P2D instructions. It also has basic DSP data processing capability that accelerate simple computation in the protocol and display of user interface processing. The features of M2R can be summarized as follows.

- RISC with single 30G set issue
- 32bit fixed instruction set
- Six stage pipeline : FE - PD - DE - E0 - E1 - E2
- Interrupt disable during instruction execution within delayed slot
- 3read-1write register file
- 2 delay slot for decode stage branch and execution stage branch and link
- 3 delay slot for execution stage branch
- 2 delay slot for load operation

Each processor core adopts a programmable dynamic clock control that balances power consumption by the complexities of protocol tracking, user interface, and DSP processing. Clock speed of each core can be programmed in a real-time in order to match a requirement of target application. Each core also provides four states to control an energy, active state, sleep state, deep sleep state and power-off state. In active state, processor can change the processor clock between normal operation clock, a half of one, and a third of one. When a program execute *idle* instruction in the active state, processor pull down the processor clock without affecting the I/O device operation. Under the sleep state, whole system clock includes processor and I/O device disabled except real time clock (RTC). Wake-up will be occurred by the RTC time-out or external trigger signal since on-chip phase locked loop (PLL) is still working in order to fast response. An extreme power saving is possible if the processor enters to the Deep sleep state, which the whole clock stopped including PLL. Wake-up from the Deep sleep states takes more latency because it requires PLL boot-up time.

Each core has independent caches to reduce memory access latency. 16 Kbytes instruction and 8 Kbytes data caches on each RISC and DSP cores, and furthermore, the DSP core have scratch-pad memory such as 48 Kbytes XMEM and 48 Kbytes YMEM [12]. On-chip data cache can be configured as copy-through or copy-back mode dependent on the section indicator of address field. In cooperate with data cache, total 96 Kbytes internal scratch-pad memory is integrated enough to support hardware FIFO for each peripheral, which results in cost-effective and low power consumption systems. Whole memories can be byte and word accessible to save a valuable internal space as general-purpose data memory. Boot-up code of the processor can be placed in diverse devices such as NOR type flash, NAND type flash, and serial EEPROM, which reduce a total cost of system by minimizing a number of memory devices.

2.4 Wireless connectivity

The GDM5104 medium access controller implements the IEEE 802.11 MAC sublayer using dedicated hardware and embedded firmware. MAC hardware implements real-time functions including data pump at transmit mode, validation check and filtering at receive mode, access protocol management, and DMA transferring of data between baseband and internal shared memory. Also, the most time critical frame such as ACK, CTS or response to CF-poll can be executed by MAC hardware itself. The embedded processor handles both Lower MAC and Upper MAC altogether as well as upper layer networking protocol such as TCP/IP. The lower MAC software handles the control of MAC hardware directly and its related lower layer of MAC protocols. It also handles the WEP hardware engine for encryption and decryption. The upper MAC software handles the BSS management, power state control, Beacon generation, data queue management, and host interface. The embedded processor runs low-layer firmware that manages the flow of command/data and upper-layer firmware to/from the application including the scan and join operations, and maintains transmit and receive queues, as well as a WEP key and engine control. Of course, the embedded CPU can control the time critical frame in the manual mode.

2.5 Peripheral interface

The GDM5104 provides various peripheral interfaces such as off-chip memory interface, host interface, PCI/mini-PCI/CardBus, ATAPI, USB, UART, PCM, I2S, SPDIF, JTAG, Flash Memory/Card, and up-to 100-general purpose programmable I/O(GPIO) interfaces. The GDM5104 has two systems bus called IMB and AMBA. The IMB bus is specialized for high-speed communication between high bandwidth devices such as CPU, USB2.0, on-chip memory, and external SDRAM. Operation clock of the IMB bus is the same as processor clock to reduce the latency for high bandwidth data. Through the superior high performance bus, the embedded processor provides a sufficient bandwidth to execute the application that requires the large size of code and high throughput data movement. For the general peripheral data communication, each block is

Table 1. Chain tools

tool	description
vincent-elf-gcc	Vincent C compiler
vincent-elf-g++	Vincent C compiler
vincent-elf-as	Vincent assembler
vincent-elf-ld	Vincent linker
vincent-elf-ar	Vincent librarian
vincent-gdb	Vincent source-level debugger
vincent-binutils	Vincent binutils
elf2flt	used to create a flat format output executable binary file
genromfs	used to create a file image for flash from a directory

connected to AMBA AHB and APB bus also, which the AHB provides higher speed than the APB.

3 Software Environment

3.1 Operating systems and tool chain

Linux is one of the prominent operating system in the embedded world. Open source kernel and rich application can be migrated into the embedded application easily, and its powerful network protocols and applications are providing the network accessibility in the embedded system. We select the uClinux operating system on the GDM5104, which is one of the variations of Linux for embedded systems. For applications that require preemptive kernel, eCos[13] on GDM5104 is under development also. Vincent Software Development Toolkits (VSDT) is a development package that includes the basic tool chain and programming software to support the RISC and DSP processors. Sparc-Solaris, x86-Linux, and x86-cygwin platforms are supported to develop applications using VSDT.

3.2 Debug support

The P2D and M2R cores have on-chip hardware debugger to support run-time debugging, and the on-chip debugger cooperates with external off-chip debuggers, GCoH and GNU debugger. JTAG, IPC, and PCI interfaces can be used as a communication channel between on-chip and off-chip debuggers. Figure 5 shows the debugging environment operates on run-time. Off-chip debugger controls on-chip debugger through the debug command register (DEBUG_CMD). Five types of commands are supported by DEBUG_CMD: SET, RUN, INTERRUPT GENERATION, RESOURCE ACCESS, and BIST commands. Special bit fields are prepared in the cores that generate internal exception for the purpose of hardware debugging only. By the value of each bit, the corresponding exception will be generated internally.

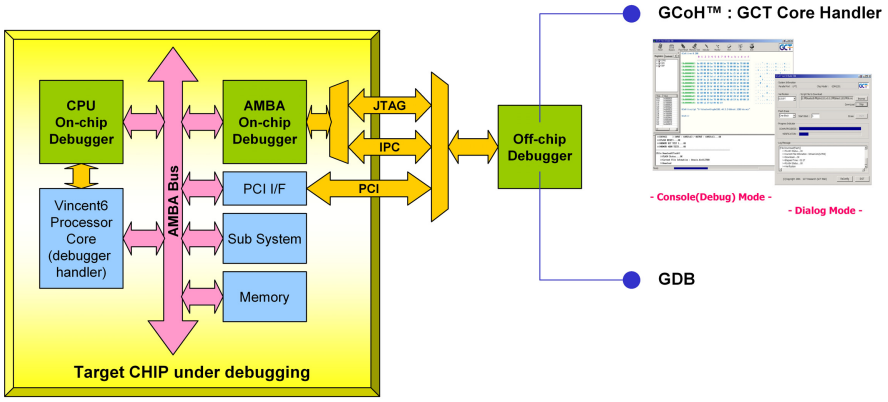

Fig. 5. On-chip and off-chip debug interface

Table 2. Performance of audio processing codecs using P2D (Mcycles/sec)

AMR		G.729AB		G.723.1 (6.3Kbps)		G.169
encoder	decoder	encoder	decoder	encoder	decoder	
25.5	4.4	21.5	3.9	29.9	2.3	15.7

By control of the external off-chip debugger, the processor cores can be configured as one of the three processor modes, which are normal run, debug wait, and debug run. Under normal run mode, the on-chip debugger only provides limited commands related with memory and non-conflict resources with processor core. Debug wait mode provides holding of execution that cooperated with the off-chip debugger. Under debug wait mode, the pipeline of the processor core is stopped but other sub-systems, such as peripheral devices, are working except timer. The timer can stop or work according to the specific configuration. Under the debug run mode, processor executes operations but the execution will be stopped at the preset counts of instructions or predefined breakpoint position by the configuration. The boot-up state of processor mode is defined by external chip interface signals, and off-chip debugger can change each mode anytime.

4 Performance evaluation

By the M2R and P2D dual core architecture, it offers unique advantages in performance and power consumption for wireless multimedia systems. The M2R is well suited for handling protocol, user interface code, OS, and applications. The P2D, on the other hand, is better suited for the real-time signal processing applications commonly used in multimedia codec. In this paper, we present several audio codec performances using P2D core as shown in Table 2. In terms of

optimization, quality of the source code is in early-stage to conclude the performance of P2D, so we expect the performance will be improved by the profiling of the code, further detailed performance will be released within near future.

5 Conclusion

Advent of the low power embedded processor pushes the digital appliances to an outdoors. The wireless technology enlarges a capability of the mobile application by its excellence of connectivity compared to wire communications. One of the most laborious obstacles is saving of the energy of mobile applications that operate using primary or secondary batteries. For the low power consumption and high computation/data-rate applications with the wireless connectivity, we integrate the high performance RISC and DSP cores with most wireless standards, IEEE802.11a/b/g and Bluetooth, on single silicon. By the seamless control of function units with high performance buses, every complicated application that require various peripheral operations, complex computations, and high-speed wireless communications can be offered using minimal power.

References

1. G. Semeraro and G. Magklis, R. Balasubramonian, D. Albonesi and S., Dwarkadas and M. Scott: Dynamic frequency and voltage control for a multiple clock domain microarchitecture Intl. Symp. on Microarchitecture (MICRO) (2002) 356–367
2. A. Iyer, D. Marculescu: Power efficiency of voltage scaling in multiple clock Proc. Intl. Conf. CAD (2002) 379–386
3. E. Macii, M. Pedram and F. Somenzi: High-Level Power Modeling, Estimation and Optimization Proc. DAC (1997) 504–511
4. Intel PXA27x Processor Family Developer's Manual (2004)
5. Brian P. Crow, Indra Widjaja, Jeon Geun Kim, Prescott T. Sakai: IEEE 802.11 Wireless Local Area Networks IEEE Commun. Mag. Vol.35 N.9 (1997) 116–126.
6. K. Brandenburg: MP3 and AAC Explained K. Brandenburg. MP3 and AAC Explained 17th Intl. Conf. High Quality Audio Coding (1999)
7. J. C. Haartsen: The Bluetooth radio system IEEE Pers. Commun. Mag. (2000) 28–36
8. H-J. Suh, H.J. Lim, J. Kim: GDM5302: Wireless Integration of a Mobile Multimedia Processor 2005 Intl. Conf. Embedded Systems and Applications (2005) 182–187
9. AMBA Specification rev 2.0 ARM (1999)
10. K. Wires, M. Schulte and J. Stine: Variable-Correction Truncated Floating Point Multipliers 34th Intl. Asilomar Conf. Signals, Circuits and Systems (2000)1344–1348
11. S. Kanthak, K. Schutz and N. Ney: Using SIMD Instructions for Fast Likelihood Calculation in LVCSR Proc. of the IEEE Int. Conf. on Acoustics, Speech and Signal Processing (2000)
12. M. Kandemir and A. Choudhary: Compiler-directed scratch pad memory hierarchy design and management 39th ACM/IEEE Design Automation Conf. (2002) 690–695
13. eCos User Guide Red Hat, Inc., eCosCentric Ltd. (2003) available on http://ecos.sourceware.org/docs-latest/