Parallel Embedded Systems: Optimizations and Challenges *

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With the advance of system level integration and system-on-chip, the high-tech industry is now moving toward multiple-core parallel embedded systems using hardware/software co-design approach. To design and optimize an embedded system and its software is technically hard because of the strict requirements of an embedded system in timing, code size, memory, low power, security, etc. while optimizing a parallel embedded system makes research even more challenging. The research in embedded systems needs integrated efforts in many areas such as algorithms, computer architectures, compilers, parallel/distributed processing, real-time systems, etc.

This talk will first use an example to illustrate how to find the best parallel algorithm and architecture for this example application, and the technical challenges on design of parallel embedded systems. Because loops are usually the most critical parts to be optimized in DSP or any computation-intensive applications, the talk will then present our results in various types of optimizations for loops in timing, code-size, memory, power consumption, heterogeneous systems, etc. Many of our techniques give the best known results available in literatures. This talk will show that using our multi-dimensional retiming technique, any uniform nested loops can be transformed such that all the computations in the new loop body can be executed simultaneously. This is the best possible result and can be applied to many applications executed on VLIW or other types of parallel systems.

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