Design of Face Recognition Door Manager System Based on DSP

Pu Dongbing[12], Du Changrui[1], Yu Zhezhou[1], Zhou Chunguang[1]

(1.Department of Computer Science, Jilin University, Changchun, 130012,China)
(2.College of Computer, Northeast Normal University, Changchun, 130024,China)
Jilin University, Changchun, 130012,China
Corresponding author: Zhou Chunguang, cgzhou@jlu.edu.cn

Abstract. This paper focuses on the design of hardware framework with DSP based on embedded face recognition door manager system including the detailed technology of circuit design among the image sensor, DSP, the door manager controller, FLASH, SDRAM, RJ45 port, timer and reset. At the same time, both the programs and algorithms are discussed in the paper. The program on face recognition has been tested on the designed board; it runs all right with fixed light condition. Not only the size and cost of the board are small, but also it is fast and highly reliable.

1 Introduction

The Digital Signal Processor (DSP) is a kind of specialized microprocessor designed for realization of digital signal processing quickly in the real time, which adopts the Harvard structure. [1] It has some good characteristics such as the convenient interface, the good stability, the high accuracy, the good reusability and convenient integration etc. [2] Along with a fast development of DSP, its function is more and more stronger, the function price ratio rises continuously, the method of development has been improved continuously, so it also quickly becomes the core component of numerous electronic products. It is extensively applied to many fields such as the correspondence electronics, signal processing, automatic control, radar, military, aviation, medical treatment, home appliances, electric power and electronics etc. On the other hand, the traditional methods of identification such as passwords, certificates, IC card etc, which often cause the falsification, theft and crack as they can be separated from the owner. They couldn't fully be satisfied with the modern social economic activities and social safety. Therefore, the personal identification system based on the human body biologic characteristic gradually becomes very well known to the society. But the traditional face recognition system are achieved depending on large-scale integrated circuits same as microcomputers, both drivers of peripherals and image capturing depended on the hardware and operating system in a computer, which result in some disadvantages such as the slow image processing, low reliability, poor function in real time etc. [3] Applying DSP and the image sensor to the body identification system with door manager system can achieve such advantages as quick speed, low cost and considerable reliability. This paper focuses on the design of hardware framework in a small face recognition door manager system, which based on DSP and image sensor. Such problems as the peripherals, interface design and the program of face recognition also have been discussed elaborately in the paper.

2 System Architecture Design

The architecture of the system is shown in Figure 1. BlackfinADSP-532 is the core of the hardware. On the other hand, the peripheral chips primarily consist of asynchronous FLASH, SDRAM, the image sensor, the door manager controller, network chip, clock, power, resets, and JTAG.

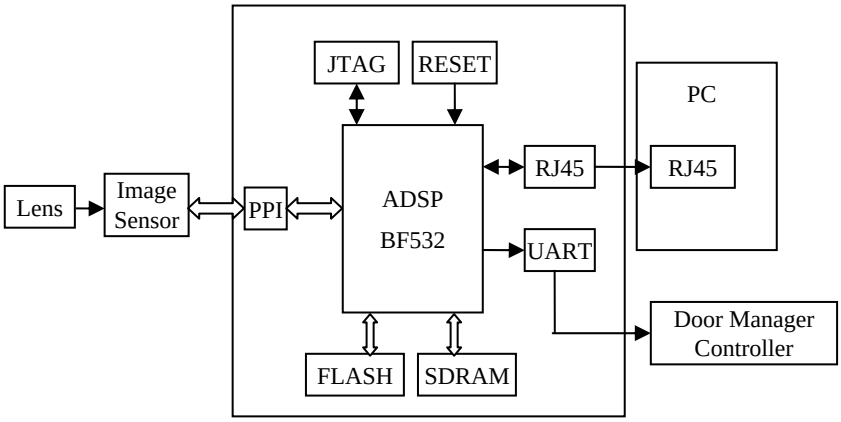

Fig. 1. Architecture of system

Firstly the system is initialized and boots along with electrifying, then it loads programs and data from FLASH to SDRAM. The data mainly includes the face detection and location template, mean face matrix, eigenface template and match template etc. When someone wants to pass the door, he or she gives an interrupt signal to the system by pressing the interrupt key. The image sensor captures the image via PPI interface under DSP controlling. Then the captured image is transmitted to the off-chip SDRAM. A feature value of person face will be achieved here when programs complete to process the image information. Since programs bring about a great deal of temporary data when obtain the feature value of person face, whereas the on-chip RAM for DSP is not enough to hold them. Thus an extended off-chip SDRAM of 4M*16-bit is added to the system. Those tasks including face detection and location, feature extraction is mainly processed in the extended SDRAM. The following task is matching the extracted feature value with data stored in the database of face feature, and calculating the threshold value of similar degree. Eventually DSP sends message to the door manager controller through the UART interface according to the similar degree threshold value. The door manager controller can send message to open the door or play warning sound. Meanwhile, the log of recognition will be stored in server-named PC through RJ45 interface. These log information can be available for management. The JTAG of the system is used for emulating, debugging on-line and updating the information of person’s face feature periodically.

3 Interface Design

3.1 Image Sensor Interface Design

In order to increase the speed of image capturing, the system adapts HDCS1020 image sensor. It can capture the image of CIF (352*288) up to 30f/s with A/D conversion itself. [4] And it can joint the data bus of DSP directly without any conflict.

Because programs of system process black/white image, so the data bus D0-D7 of image sensor connects with the PPI pins of DSP. DSP's GPIO pin can imitate the I2C protocol to control the image sensor.[5] Figure 2 shows the way of connection between DSP and the image sensor.

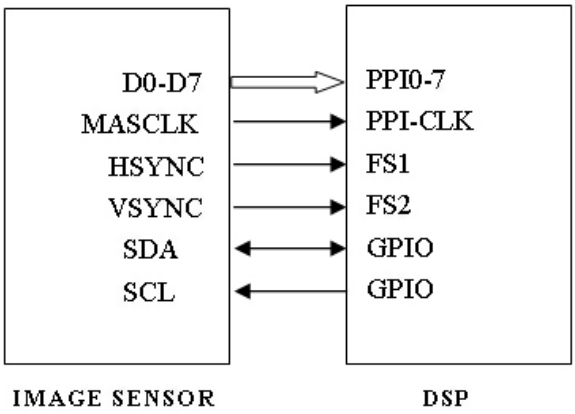

Fig. 2. Connection between image sensor and DSP

The control signals sent by DSP include two parts: address codes and control signals. Address codes are used to select the image sensor, and control signals perform the initialization and image capture. Control signals include beginning signal, response signal and ending signal. Beginning signal shows that SCL is high Data begin to be transmitted when SDA jumping from high to low. The image sensor sends response signal to DSP when it has already received 8-bit data. DSP sends signals to the image sensor and waits until response signals from the image sensor arriving to decide whether continue signal from it. When SCL is high and SDA jumps from low to high, DSP sends the end signal. Figure 3 shows the scheduling of I2C bus protocol. [6]

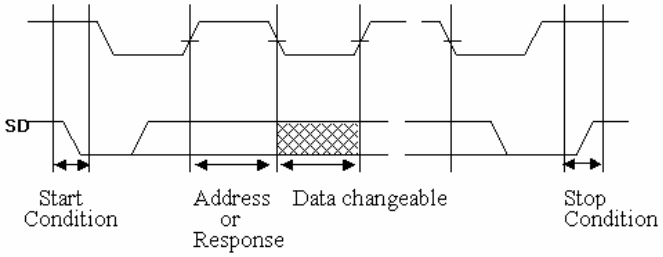

Fig. 3. Scheduling of I^2C bus protocol

3.2 FLASH Design

DSP uses a 16-bit EMIF loading model. In this model, pins of BOOTM [1:0] are set to 01. The boot kernel in the on-chip Boot Rom loads the programs and data from FLASH to SDRAM, and then the

system begins to run.[7-8] The address corresponds to the BANKO space of DSP, so we connect $\overline{CE}$ of FLASH to $\overline{AMSO}$ of DSP. As the programs and data are enormous, we added an extended 4BANK*512K*16-bit of FLASH to the system. $\overline{AMSO-3}$ pins of DSP respectively connect to $\overline{CE}$ pin of four FLASH chips. A[19..1] are address lines of DSP, they are connected corresponding to A[18..0] of FLASH which is shown in figure 4. 4MB spaces of FLASH can be enough to hold system program, data and face feature templates of about 1000 persons.

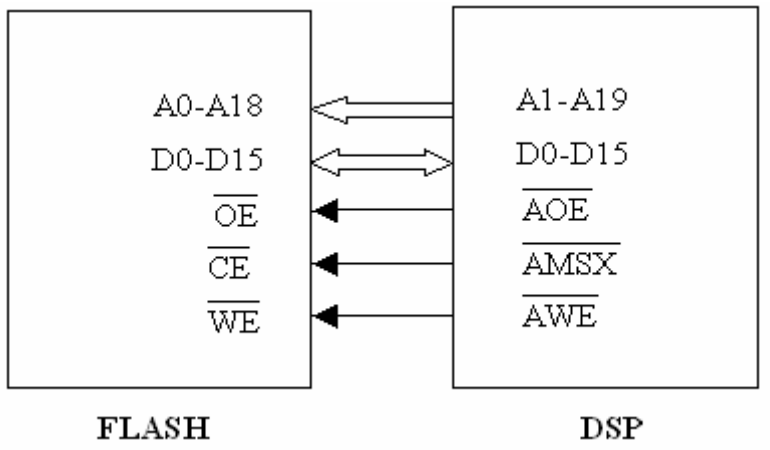

Fig. 4. Connection between FLASH and DSP

3.3 SDRAM Design

In order to provide a bigger space for programs and data of the algorithm, an extended 4M*16-bit of SDRAM is added to the system. As the row and line address are reusable for Blackfin, its connection way is greatly different from DSP 54X series of T1. The connection way for boundary/row and column address is shown in figure 5. The row selecting $\overline{SRAS}$, column selecting $\overline{SCAS}$ and writable signal $\overline{SWE}$ of DSP are directly connected to the corresponding pin of SDRAM. A1-10, A12 and A18-19 address bus of DSP are respectively connected to A1-10, A11 and BA0-BA1 of SDRAM; SA10 and SDQM0-1 of DSP are connected to A10, DQML and DQMH of SDRAM respectively.[9]

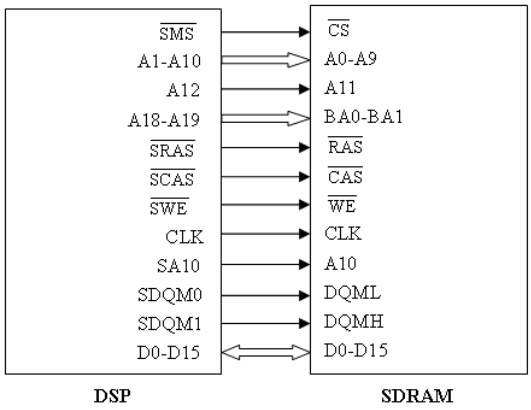

Fig. 5. Connection between DSP and SDRAM

3.4 Corresponding Interface Design between DSP and PC

The LAN91C111 network chip is built in the hardware of our system. It is 3.3v MII (media independent interface) integrated the MAC+PHY on-chip and 128 pins QFP package. [10] The

LAN91C111 integrates the IEEE802.3 Physical Layer (PHY) and Media Access Control (MAC) into the same silicon. The data path connection between the MAC and the internal PHY is provided by the internal MII. The LAN91C111 also supports the EXT-PHY mode for use of an external PHY. It provides a flexible slave interface for easy connectivity with industry standard buses. The Bus Interface Unit (BIU) can handle synchronous as well as asynchronous transfer, with different signals being used for each one. The total internal memory FIFO buffer size is 8k bytes. These properties are satisfied to the system request. The TJ45 adopt HFJ11-2450s chip. The system bus is 16-bit. So the $\overline{ABE0\text{-}1}$ pins of DSP connect to the $\overline{NBE0\text{-}1}$ pins of network chip. $\overline{NBE2\text{-}3}$ connects to high impedances. The hardware connection is shown in figure 6.

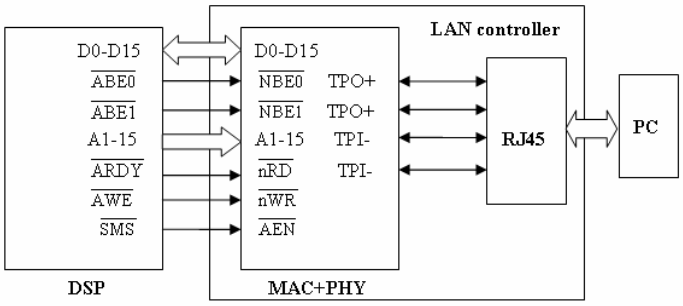

Fig. 6. Connection between DSP and LAN controller

3.5 Other Peripheral Circuit Design

In order to provide real-time debugging for program in DSP, we connect JTAG with the emulator in our system. Furthermore, it also can be used to burn data and programs to FLASH. The periodical update task of face feature information is also completed by JTAG.[11-13] The UART interface is the equipment between DSP and the door manager controller, which can send message to open door or play warning sound.

The power equipment of system is TPS70302PWP. It can supply double adjustable voltage. One is 3.3V for peripheral circuits; the other is 1.2V for the kernel of DSP. To avoid destroying DSP by error of incorrect electrifying sequence, the system supplies electricity with peripheral circuits at first, and then DSP. The automatic and manual reset signal outputted by the power source do logical 'AND' operation before they are connected to DSP and peripheral circuits so as to reset system automatically or manually when the supplied voltage of system is too low. To prevent from the disturbance of high frequency caused by the high clock frequency of peripheral circuit, which can reduce the stability of system, peripheral clock circuit supplies 20MHz clock for DSP to match its kernel clock by PLL of DSP.[7]

4 Software Design

Firstly, the system will be initialized as soon as it is power on. Whenever someone passes the door, he or she can press the specified key to send interruption signal system. The system will mask the external interruption when it received the signal, and then it sends instructions to the image sensor to capture an image. The image sensor will notify DSP through interruption that the capture operation ends when it has completed to capture an image. Then the system starts to process the image and recognize. Finally

it gives the recognition result and opens the door in so far as right or gives a warning message (the speaker is beeping) for wrong. Figure 7 shows the main flowchart of our system.

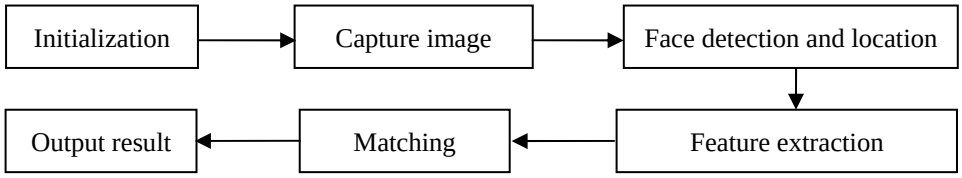

Fig. 7. System main flowchart

During the system initialization, DSP reads data from pm, mean, facetpl, eyetp1, and then store them in the variable of Pm, Mean, Facet, Eyet respectively for the following feature extraction to use. The data of captured image are stored in the fdata variable. The image sensor can capture the image without any software; it is different from the existing system in which the captured image should be converted through A/D before processing. The captured image of face will be performed unitary operation on size and gray degree. The following step is to judge whether there is a face existed in the picture and give the accurate location if a face existed. Program locates such parts of the face as head, face, and eyes pupils. The flow chart is shown in figure 8.The method of detection and location in our system is based on the traditional template matching, and it is used for those images, which are static and gray, captured under simple background and even shine. The result will be better if the image is positive face picture.[14-15]The method of traditional template matching is to calculate the Euclidean distance between the captured image matrix and the face template(or eye template).

After the location, the feature extraction is beginning. Firstly the data of face location subtract the data of even face stored in Mean, and then an array can be generated, the array is projected at the feature face matrix pm to extract the feature value. The method of feature extraction and selection in our system is PCA (Principal Component Analysis). [15-17]

Then program matches the extracted feature value with those templates that have been trained and stored. The algorithm for matching is NNA (Nearest Neighbor Algorithm). [18-19] In addition, the face and eye templates for detection and location, the feature face template for extracting the feature value and the match template for matching are all trained and generated in PC beforehand and burned to the FLASH of our system. The match template is composed of the face feature value so that FLASH can accommodate more people’s feature value in the limited space.

The maximum count of studying & training samples is 5 to 8 for every person. These samples have been appended in out system by generating image so as to improve the rate of recognition.[20]The sample is generated and append by a series of transformation. The main transformations are mirror transformations; rotate transformations of the picture and the changing of gray information of bottom for an image.

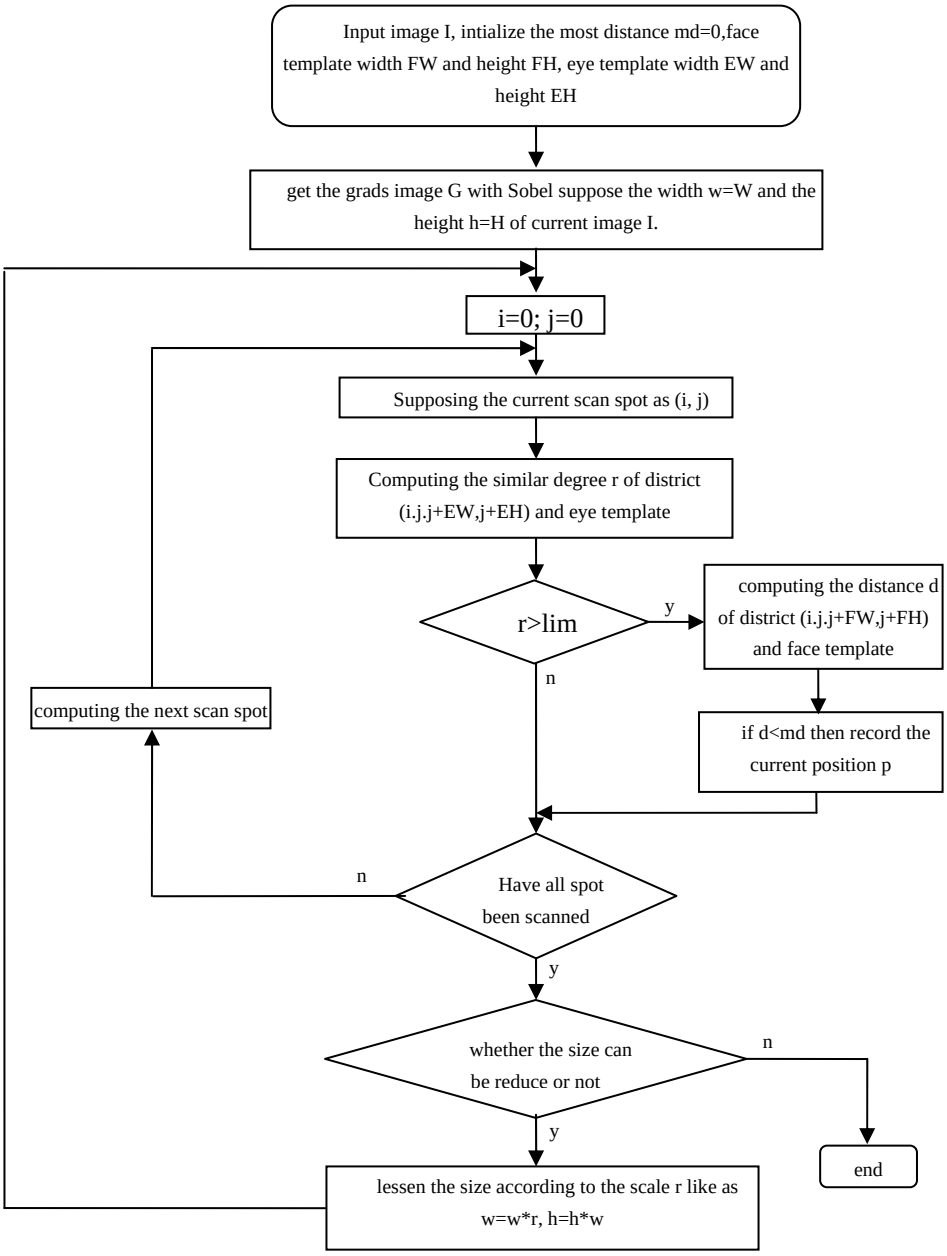

Fig. 8. Flowchart of detection and location

The most important aspect in the whole system is to select the threshold value of similar degree. The similar degree of our system is measured by cosine angle of two eigenvectors.[21] The threshold value determines the safety and efficiency of our system. If the threshold value is too high, those people who have the right to pass the door can't pass it; on the contrary, if the threshold value is too low, the reliability of system is reduced, as a result, those people who have not the right to pass the door can pass it. There are two factors to judge whether the similar degree threshold value is good or not. One is the mistake-passing rate; another is the mistake-refusing rate on the threshold value. Generally, both of factors are restricted mutually. If the mistake-passing rate were low, the mistake-refusing rate would be high. If the mistake-refusing rate were low, the mistake-passing rate would be accordingly high. The

curve in Figure 9 shows the variation of the mistake-passing rate and the mistake-refusing rate following the variation of the similar degree threshold value.

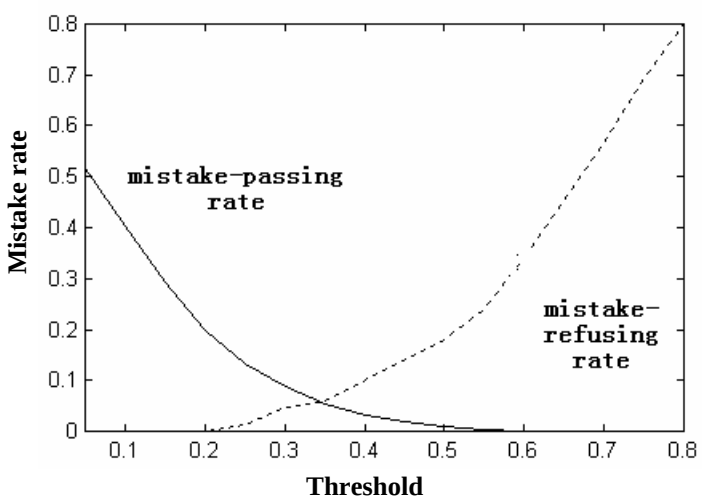

Fig. 9. Variation of the mistake-passing rate and the mistake-refusing rate following the variation of the similar degree threshold value

Figure 10 shows the results of our system.

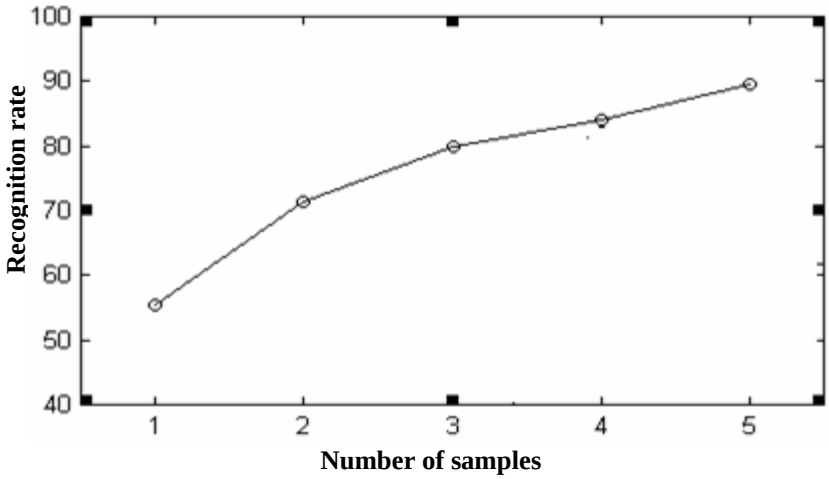

Fig. 10. Result of Recognition in system

5 Conclusion

In this paper, we have designed a hardware framework, which based on the face recognition of door manager requirement. DSP is the kernel of the door manager system and face recognition algorithm has been applied in it. We have implemented the hardware interface circuit design of the system and the algorithm testing. The result is good under the still light. In the same time, the system integrates image sensor, DSP, FLASH, network chip and other peripheral equipments on a single board. Not only it is

smaller in size, lower in cost, but also it can work faster and more reliably. In a word, it will be applied in many fields in the future.

Acknowledgement

This work was supported by the National Natural Science Foundation of China under Grant No.60433020, and the Key Science-Technology Project of the National Education Ministry of China under Grant No.02092.the Key Laboratory for Symbol Computation and Knowledge Engineering of the National Education Ministry of China.(93K-17).

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