Development of a Microdisplay Based on the Field Emission Display Technology

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Abstract. We have been developing a microdisplay based on the field emission display (FED) technology, which is advantageous in power consumption, image quality and long term stability. We have adopted LSI-driven anode pixels, which enables active-matrix addressing and, therefore, highly precise and high-quality microdisplay. The structure was optimized according to the simulation study of electric field and electron trajectories. The driver LSI has been designed, evaluated by simulation, and the wafers have been produced. Anti-crosstalk grid should be constructed on the LSI by photolithography and the relevant study has been performed.

1 Introduction

Microdisplays are defined as microminiaturized displays typically with screen size less than 1.5" diagonal. They are used in wearable displays, in the traditional viewfinders of digital cameras and in mobile communication instruments such as cellular phones. While ubiquitous instruments are expanding in our life, demand for the microdisplay is rapidly increasing.

In Table 1, technologies to realize microdisplays are shown. Although the cathode ray tube (CRT) display provides high image quality, it is not regarded as most suitable for microdisplay due to its large power consumption and size. The liquid crystal display (LCD), which is the most widely used flat panel display (FPD), is also not most advantageous in power consumption and volume because it needs a backlight. The Organic LED (OLED), recently emerging as a thriving technology for flexible FPDs, is still on its way to overcoming the short lifetime. It can be suitable for cellular phones since many of customers replace their cellular phones to new products frequently. Microdisplays for the wearable displays, however, would be required to have enough endurance especially when they are subjected to outdoor uses. The field emissions display (FED) is expected to involve high image quality of CRT, small volume, low power consumption and long term stability. Therefore, we have chosen the FED technology to develop a microdisplay.

Table 1. Microdisplay technologies compared to our method (FED). Comparison is made for XGA (1024×768 pixels) displays. The latest models in 2003 are referred except for the FED.

Technology	Voltage	Power Consumption	Light Emission	Size ($W \times L \times H$ [mm])
CRT	high	1500mW	self-emissive	$30 \times 75 \times 19$
LCD	low	900mW	backlight	$40 \times 38 \times 19$
OLED	low	300mW	self-emissive	$26 \times 20 \times 10$
FED	low	50mW	self-emissive	$26 \times 23 \times 5$

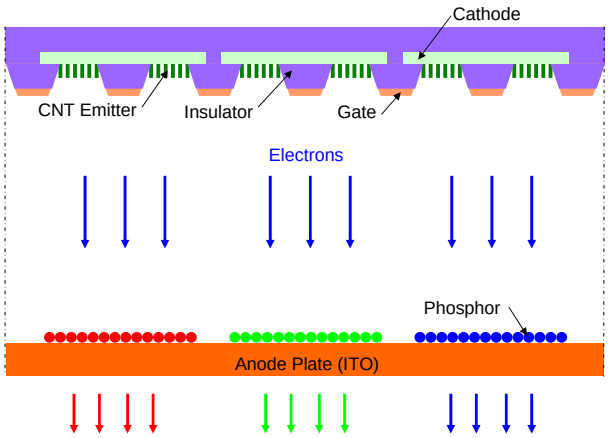
2 Structure of the Field Emission Microdisplay

Fig. 1(a) shows the most commonly used structure of the FED. Electrons are emitted from field emitters that are arrayed in pixels on a cathode plate. Carbon nanotubes (CNTs) [1] are often used as the field emitters because their high aspect ratios, good chemical stability and high mechanical strength are thought to be most suitable for stable field emitters with low threshold voltage in FEDs [2]. The emitted electrons collide with the phosphor painted on the anode plate and cause electron-beam induced emission of light. The electron current of each pixel is controlled by voltages of the gate and cathode electrodes which cross at that pixel.

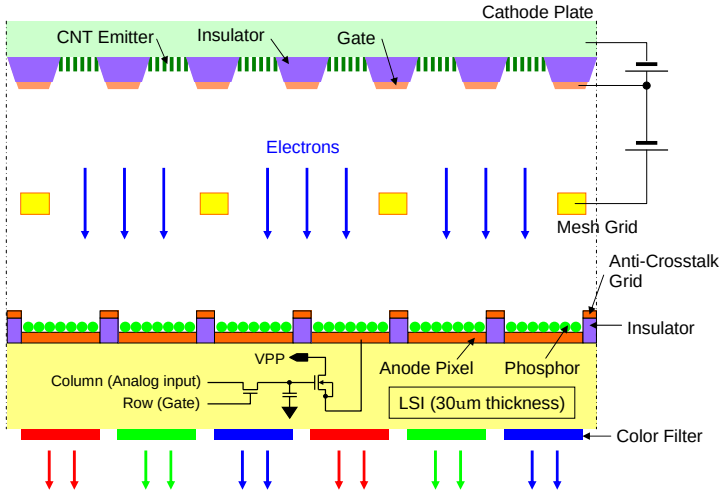
The structure design of our microdisplay is illustrated in Fig. 1(b). Here, CNTs are put on one cathode plate and applied same voltage. The gate voltage is also fixed at one value. The CNTs, the gate and the mesh grid compose a triode structure, which introduces field emission from the CNTs. The electrons go through the mesh grid and reach the [ZnO:Zn] phosphor painted on the anode pixels, which consist of surface metal of a CMOS LSI. The brightness of each pixel is determined by the anode voltage, which is controlled by the pixel driver LSI. Additional grid electrodes are necessary between the pixels such that crosstalks should be suppressed. The emitted light transmits through the LSI, because the LSI is grinded to the thickness of about 30μm, and filtered by the red, green and blue color filters.

The most characteristic point of this structure is that the brightness is controlled by the anode pixels. This method has following advantages:

1. Active-matrix addressing is possible because the driving LSI is free from thermal damage caused by CNT synthesis. The cathode-driven FED, in which passive-matrix addressing is usually used, often suffers from parasitic-capacitor induced crosstalk.
2. Driving voltage is small and therefore the production cost can be decreased. In the case of the cathode-driven FED, large voltages applied to the gate and the cathode must be driven.
3. The cathode just provides uniform distribution of electrons and needs not to be focused. On the other hand, electrons in the cathode-driven FED must be focused onto the facing anode pixel, and the focus ability limits down-sizing.



(a)



(b)

Fig. 1. (a) The structure of the most commonly used FED design, where the brightness of each pixel is controlled by the anode and gate voltages. (b) The structure of our field emission microdisplay, where the pixel brightness is controlled by the anode pixels.

4. Since the cathode does not have pixel structure, precise alignment between the cathode and the anode is unnecessary and the production process can be simplified. In addition, the anode and the cathode can be developed individually.

3 Simulation of Electric Field and Electron Trajectories

In order to design the structure shown in Fig. 1(b), we have investigated electric field and electron trajectories for various candidate structures using the two-dimensional finite element method (FEM) software package, "TriComp". The examined models are illustrated in Fig. 2. Distance between cathode and anode plates is supposed to be 500μm for the models A and B, and 1000μm for the models C and D. For the models C and D, a floating mesh grid is inserted in the midst of between the cathode and anode plates. The pixel size is supposed to be 8μm width and the grid width to be 2μm. Since the LSI is produced by a 16V process, the maximum amplitude of the anode voltage is about 15V, where the CMOS threshold voltage of about 1V is subtracted.

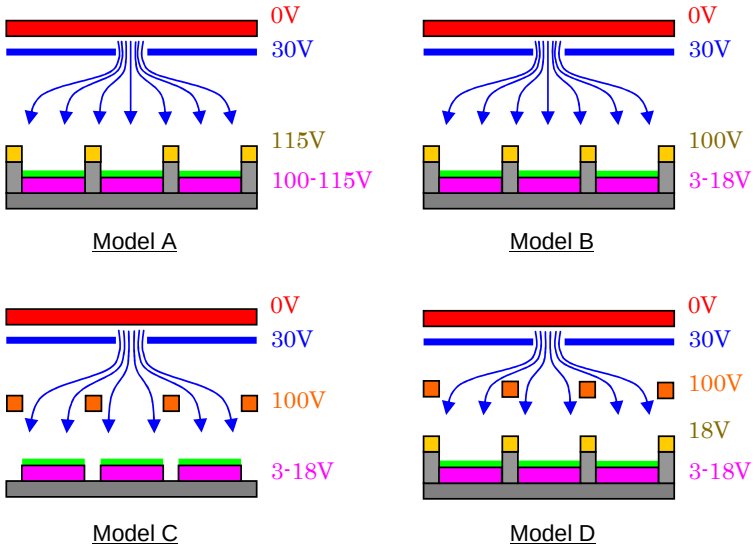


Fig. 2. Models used in the simulation of electric field and electron trajectories.

In the model A, the anode LSI chip is biased 100V higher than the cathode so that the cathode CNTs can be applied enough field. In this case, energy of arriving electron only differs by 15%, i.e. between 100eV and 115eV. In addition, the simulation has shown that the change of the number of electrons is also very small. Therefore, we cannot expect enough contrast for this model.

In the model B, in order to circumvent the above problem, the minimum voltage of the anode pixel is set 3V higher than the cathode voltage so that the minimum-energy electrons reach the phosphor with its emission threshold energy of about 3eV. On the other hand, the on-LSI grid is set to 100V, which is necessary for the electron emission by CNTs. Here, electrons are accelerated towards the on-LSI grid and then decelerated towards the anode pixels. In this model, many part of electrons were found to be absorbed in the on-LSI grid or collide with the sustaining insulator because of strong field generated around there and may cause a charge-up problem.

The model C has been suggested so that the charge-up is suppressed by separating the grid from the LSI. However, the model C suffers from crosstalk between pixels because of absence of the on-LSI anti-crosstalk grid.

Finally, we propose the model D, the double grid structure. The simulation result based on the model is shown in Fig. 3. As can be seen, the number of electrons arriving the insulator is small enough (about 9% of emitted electrons). Fig. 4 shows the change in the number of electrons arriving the anode pixels according to the anode voltages. Here, the left pixel voltage is fixed and the right pixel voltage is swept. Changes observed on the left pixel, as shown in Fig. 4(a), are flat within the size of statistical error and indicate that the crosstalk between the neighboring pixels is small enough. It is found that the on-LSI grid should be set taller than the phosphor surface in order that the grid works well. The smooth increase for the right pixel, shown in Fig. 4(b), would help deep contrast and good linearity of brightness against the applied voltage.

4 Design of the Driver LSI Chip

The LSI chip to drive the anode pixels is designed based on the high-voltage 0.6μm CMOS technology. The device provides a matrix output of open-source high-voltage N-channel MOSFETs and is equipped with 352×240 pixels on its face. The analog and digital power supplies are both 16V and the clock speed is 7.16MHz. Each pixel has a size of $30 \times 33\mu$m and consists of three sub-pixels, as can be seen from the pixel layout in Fig. 5(a). Larger area is devoted to the red pixels than others because the red light would be weaker than green and blue lights after passing the color filters. The sub-pixel circuit component is illustrated in Fig. 5(b). The analog voltage is supplied from the COL* input at the certain clock period scheduled, and held in the capacitor by the latch signals ROW* and ROWX*. During the frame period of 32ms, the held voltage is applied to the anode pad via a source follower. The droop is designed to be less than 20% of the held voltage during the frame period.

The Fig. 6 shows the block diagram of the driver LSI. The analog data for red, green and blue sub-pixels are fed in parallel into the column registers. The column resisters COL1 to COL352 are opened in turn according to the CCLK with the period of 140ns. Then, the signals are gated by the row register outputs ROW(X)1 to ROW(X)240, which are controlled by the RCLK with the period of 63.5ns.

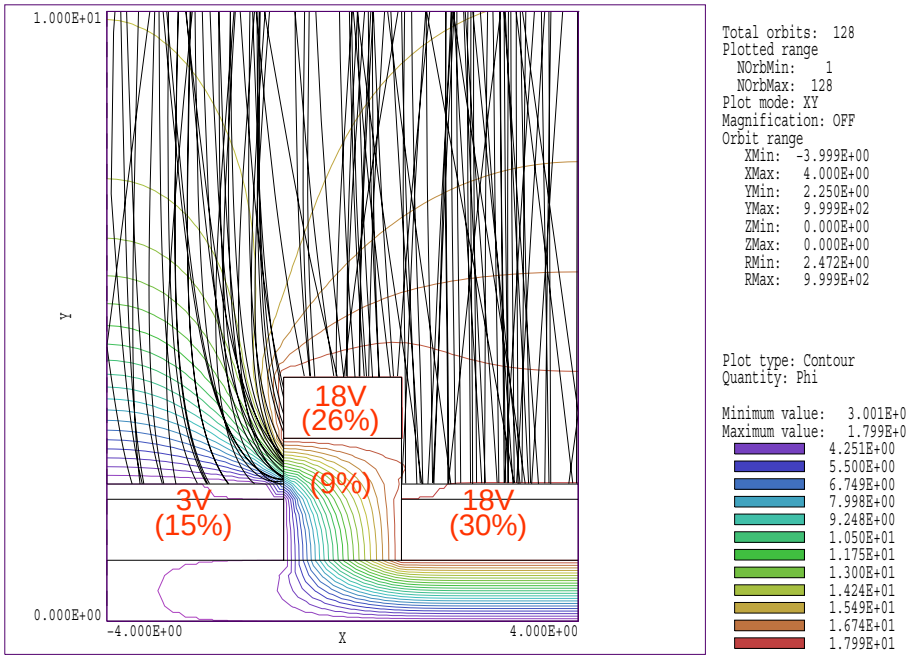


Fig. 3. Field and electron track simulation results based on the model D when the left pixel is set to 3V and the right pixel to 18V. The grid is set to the same voltage as the maximum allowed voltage for the pixels. Only around the LSI surface is shown. Also shown are the ratio of the number of electrons against the total generated electrons.

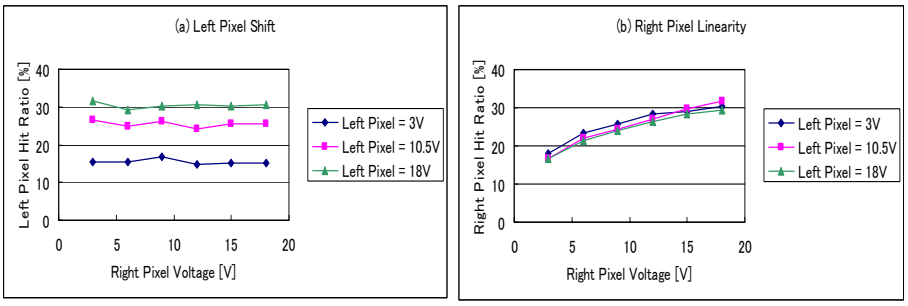


Fig. 4. Estimation of crosstalk between neighboring pixels based on the model D.

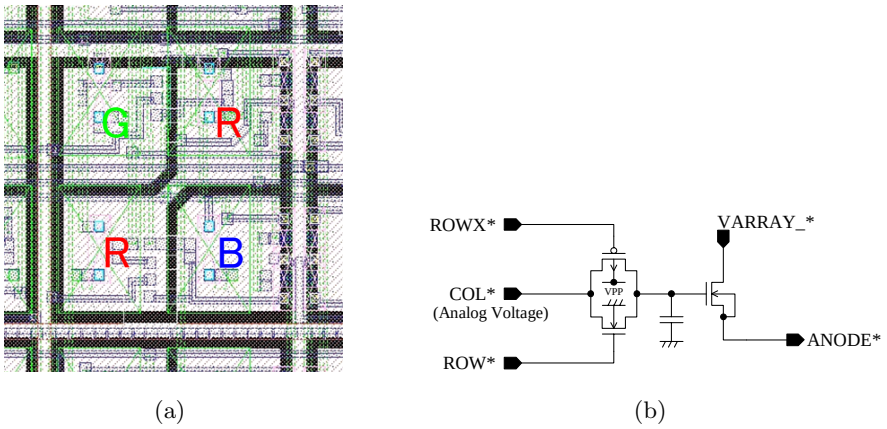


Fig. 5. (a) The pixel layout design and (b) the sub-pixel circuit component

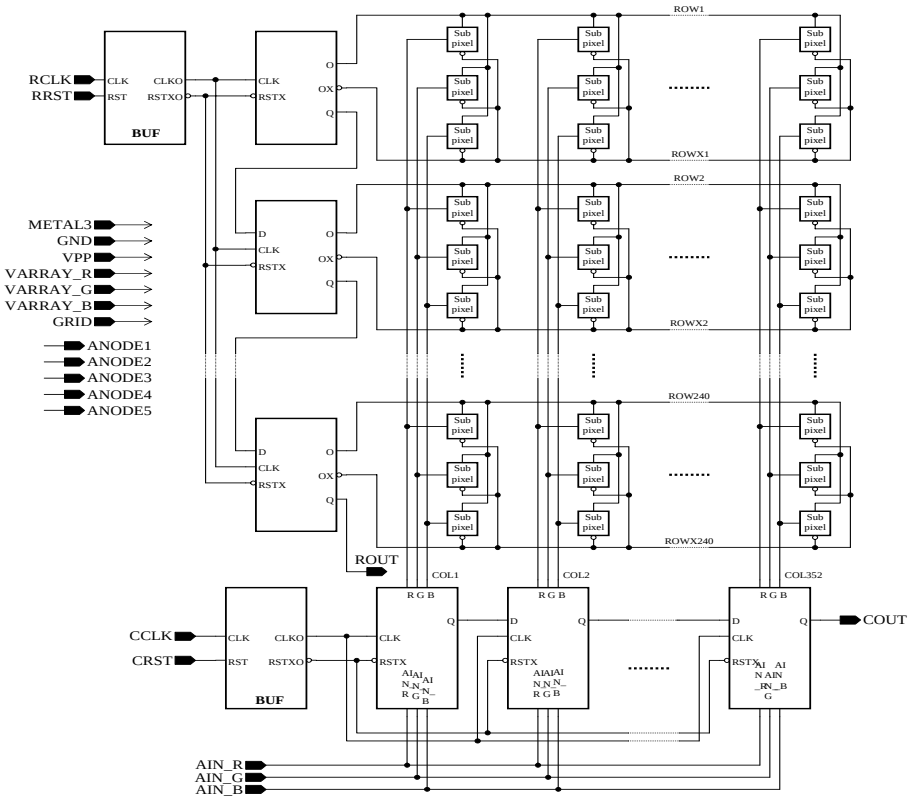


Fig. 6. The block diagram of the driver LSI.

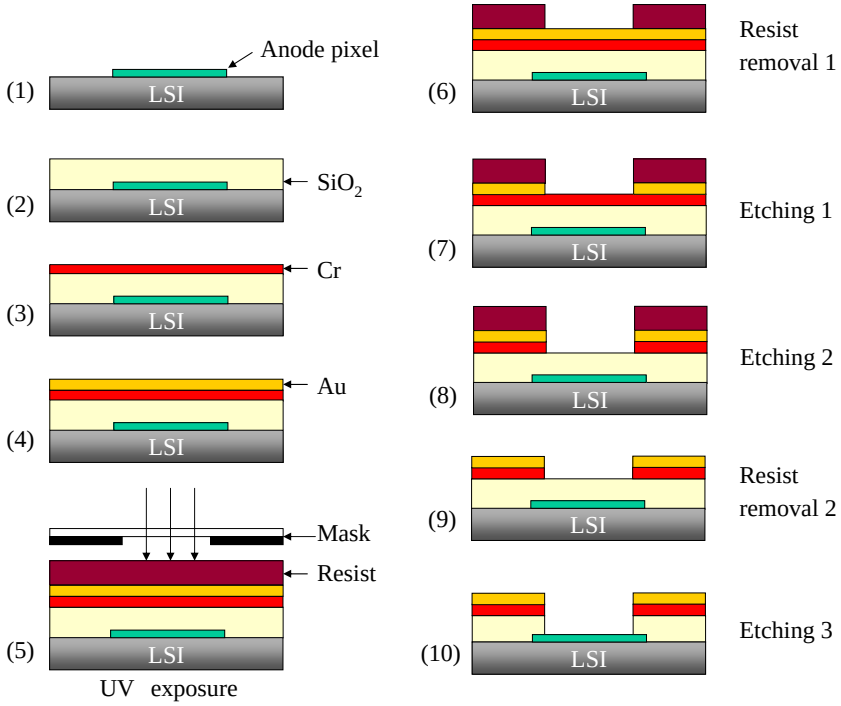


Fig. 7. The anode process to create the on-LSI anti-crosstalk grid.

The design has been submitted to the LSI processing company and prototype wafers have been delivered. We are now preparing for evaluation of electrical properties of the chip.

5 Post-Processes on the Anode LSI

As described in Section 3, anti-crosstalk grids need to be placed between the pixels together with insulator pillars underneath. The process to construct the grid structure is shown in Fig. 7. On the LSI chip (1), a SiO_2 layer is created by the thermal CVD method (2), and Cr and Au films are coated on it by spattering (3)-(4). Here, the Cr layer is interleaved as glue so that the Au would not peel off when resist is removed afterwards. Next, photo-resist is coated on the Au layer and patterned by photolithography (5)-(6). Then, the Au layer is patterned by wet etching (7) followed by the Cr etching (8) and the resist is removed (9). Finally, the silicon-oxide layer is patterned by dry etching with the metal layers used as a mask.

For the purpose of test, we have first tried the above process on a small silicon piece substrate. The scanning electron microscopy (SEM) image of the piece observed after the process (9) is shown in the upper left picture in Fig. 8.

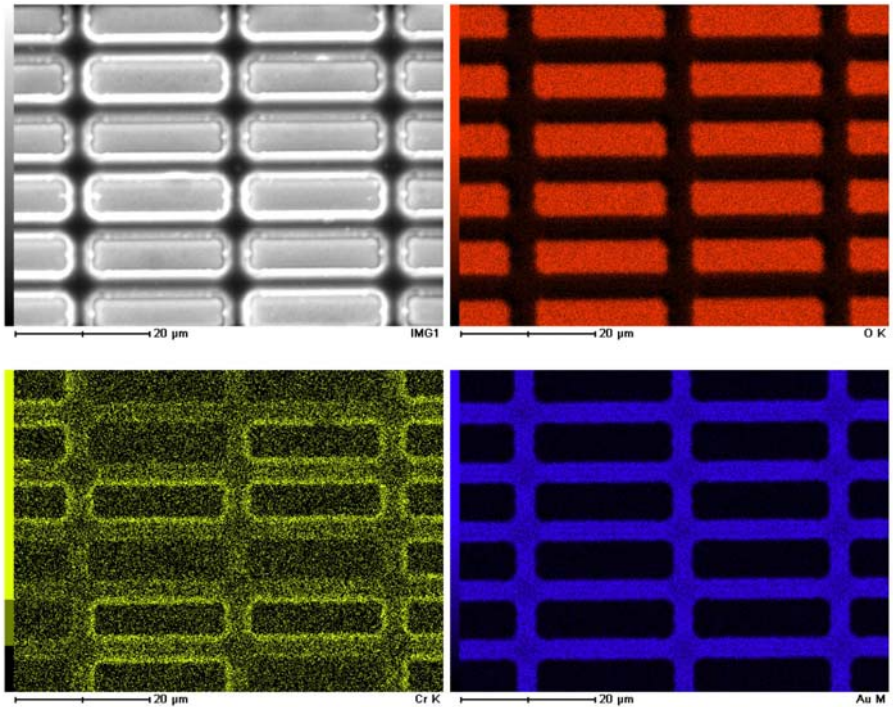


Fig. 8. The SEM image of the test piece after the resist removal (upper left), EDS mapping images of oxygen (upper right), chromium (lower left) and gold (lower right).

Note that, for the purpose of investigating the minimum possible grid width, the pattern used here is different from the one for the target LSI.

In order to confirm the right patterning of each layer, energy-dispersive spectroscopy (EDS) mapping has been performed. The upper right picture in Fig. 8 shows the EDS mapping image of oxygen, which actually indicates the SiO_2 image. Here, since the SiO_2 layer is shaded by the lattice-shaped upper layers, only the X-ray coming through the windows are observed. The lower-left picture illustrates the image of the Cr layer, which seems to be etched as designed, though the contrast is worse due to the X-ray absorption by the upper Au layer. The lower-right picture shows the image of the Au layer, which is also found to be patterned as designed.

6 Summary and Future Development Plans

We have been developing a microdisplay based on the FED technology with the anode-driven method. The structure was optimized by the simulation study of electric field and electron tracks. The double grid structure was found to be the

best. The driver LSI was designed and the prototype wafers were produced. Their characteristics are to be evaluated soon. The anode post-process for construction of the on-LSI grid was proposed and evaluated using a small Si piece, which is imitation of the LSI chip. We will soon test the process using the real LSI chip. Patterning of the phosphor should also be developed. In addition to the studies introduced in this paper, we have been investigating about the CNT cathode. Accordingly, construction of the complete microdisplay system will be realized in the near future.

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